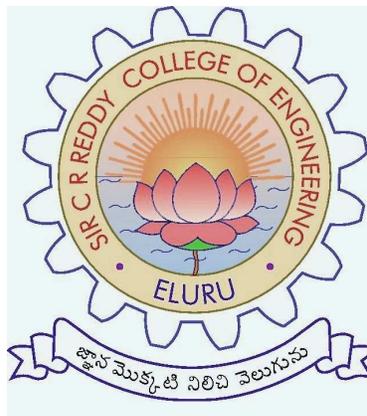


**SIR C.R.REDDY COLLEGE OF ENGINEERING
ELURU-534007**

Department of Electronics and Communications

**DIGITAL COMMUNICATIONS Lab Manual (ECE - 416)
IV / IV B.E (ECE), I – Semester**



**SIR C.R.REDDY COLLEGE OF ENGINEERING
ELURU-534007**

LIST OF EXPERIMENTS

- 1. Analog Signal Sampling & Re- Construction**
- 2. Pulse Amplitude Modulation & Demodulation**
- 3. Pulse Width Modulation & Demodulation**
- 4. Pulse Position Modulation & Demodulation**
- 5. Analog Time Division Multiplexing & Demultiplexing**
- 6. Pulse Code Modulation & Demodulation**
- 7. Differential Pulse Code Modulation & Demodulation**
- 8. Delta Modulation & Demodulation**
- 9. Amplitude Shift Keying Modulation & Demodulation**
- 10. Phase Shift Keying Modulation & Demodulation**
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- 12. Frequency Shift Keying Modulation & Demodulation**

ANALOG SIGNAL SAMPLING & RECONSTRUCTION

AIM

To study Analog Signal Sampling & Reconstruction Process.

INTRODUCTION

Pulse Modulation is used to transmit analog information, such as speech signal. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only as pulse amplitude, pulse width or pulse position, together with any synchronising pulses that may be required. At the receiving end, the original waveform is reconstructed from the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation or Frequency Modulation, the resulting receiver output can have good replica of input signal with low or moderate distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be infinitely variable, while in the later a code which indicates the sample Amplitude to the nearest predetermined level is sent. Analog Signal Sampling and Reconstruction is an analog communication method which is discussed in the following section.

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz (Frequency and Amplitude variable)
2. Synchronous Clock Generator 8 kHz output and 1KHz input.
3. ASSR Modulator
 - a) Sample and Hold
 - b) Flat - Top Sampling
4. ASSR Demodulator consisting of
Low Pass Filter (3.4 kHz cut off) and Amplifier.
5. Built-in power supplies $\pm 12V/350$ mA, $\pm 5V/350$ mA.

CIRCUIT DESCRIPTION

1. AF SIGNAL GENERATOR

The AF Signal Generator is designed around the popular Function Generator IC 8038 . The required range 200 Hz to 2 kHz is covered in a single range with one capacitor at pin 10. The Sine wave output is available at Pin 2, its symmetry is adjusted by a preset Pot of 10k, while the frequency is set by the P_1 Potentiometer 100k. Two amplifiers with +1 and $\cong -2$ gain in cascade act as buffers designed around TL084. The output amplitude is settable by the 1k Pot P_2 .

2. 8 KHz SYNCHRONOUS CLOCK GENERATOR

This is designed around a PLL IC 565 and a Binary Counter 74163. In order to enable the viewing of the ASSR Pulse stably on an Oscilloscope with respect to the analog signal, a high frequency clock (8 times the AF signal frequency) is generated using a VCO which is tuned to 16 kHz using a 100k pot provided between pins 8 and 10 of IC 565. When no signal is fed to the VCO, a chain of four FFs divides the 16 kHz to give 1 kHz output, which is fed back to the phase detector input at Pin 5 of 565.

The first Flip Flop output at Pin 14 yields 8 kHz frequency which is synchronous to the 1 kHz AF input. This is used as Sync. Clock in both modulator and demodulator.

3. ASSR MODULATOR

The ASSR modulator is designed around two Analog Switches (CD 4051) and Monostable Multivibrators using 555 ICs. A provision is made to observe Sample and Hold and Flat - Top Sampling of the ASSR Signals.

The AF input is given to a unity gain buffer amplifier connected to an Analog Sampling Gate. The gate is controlled by switching pulses from a Monostable Multivibrator (555 IC) whose pulse width is set by potentiometer P. The Synchronous Clock provides the trigger pulses. The Monostable Multivibrator generates narrow pulses at the negative edge of the Synchronous Clock.

a) SAMPLE AND HOLD : The input signal is tracked during the pulse width and held at the last level till the next pulse . In this mode the pulse width is adjusted to minimum instantaneous Sampling and Hold functions are activated. The S and H output can be Demodulated to get back the AF signal.

b) FLAT TOP SAMPLING : The Sample and Hold signal is again sampled after the first sample period. That is why the first Monostable pulses trigger second Monostable (555 IC) which has a fixed pulse width.

The second buffered Sampling gate is Sampled by the pulses which are generated after the first sample period which is in the hold period irrespective of the pulse width sample. Therefore during the output of the second sampling gate the output is always a Flat Top sample. This is another form of ASSR which can be Demodulated using a filter and amplifier.

4. ASSR DEMODULATOR

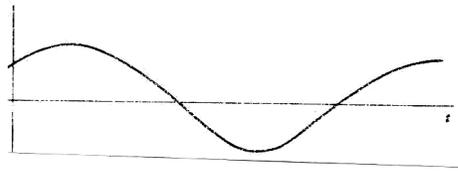
The ASSR Demodulator consists of an Allen Solly second order Low Pass Filter preceded by a unity gain buffer and followed by a pre settable gain amplifier (TL 084.)

EXPERIMENTAL PROCEDURE

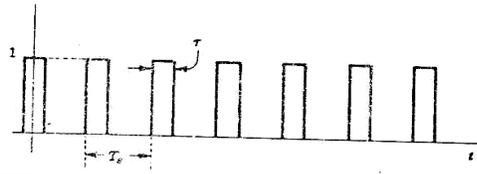
1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Observe the AF signal generator output in an Oscilloscope .It is a sinewave of frequency varying from 200 Hz to 2 kHz with 0-5V p-p Amplitude variation. Adjust the frequency to nearly 1 KHz,with the help of Potentiometer P_1 .
3. Observe the output of the 8 kHz Sync. Clock generator. Its frequency can be varied using 100k trim Pot. Adjust its free running frequency such that Sync. Clock output is almost around 8 kHz
4. Connect the output of the AF signal generator to the 'Sync. Signal input' of the Sync. Clock generator shown at dashed line . Observe that both the signals are synchronised on the Oscilloscope. For this purpose feed the AF signal to Ch.1 of the Oscilloscope and the sync. Clock output to Ch 2 of the Oscilloscope. Select the trigger source as CH1 and observe that both the signals are locked. Otherwise slowly adjust the AF signal frequency on either side of 1 kHz to get the frequency lock.
5. Connect the 'AF output' of AF signal generator to the 'AF input of' the ASSR Modulator .
6. Connect the AF signal input in CH1 and Synchronous Clock in CH2 of the Oscilloscope. Choose the trigger to CH1 .Both the signals will appear Synchronised.
7. Now observe ASSR pulses with Natural Top Sampling i.e., the top of the pulses will follow the input signal during the sampling period. This output can be given to Demodulator and the Demodulated output can be seen as replica of the AF output.
9. The effect of variation in AF frequency and amplitude can be studied at the output.
10. Alternately, the frequency and amplitude of the AF signal is brought back to 1KHz .
11. The sampled output will be a Stepped sine wave whose amplitude is held constant for the rest of the period after the sampling pulse.
12. This is also a form of ASSR which can be Demodulated and seen at the Demod output.
13. Now connect the CH2 of the oscilloscope to Flat Top output. We observe Flat Top ASSR pulses which are in the post sampling period.
14. Connect these pulses to the Demodulator and observe the Demod output.
15. Thus the trainer is useful in observing S&H ASSR pulses and Flat Top ASSR pulses at different frequencies and amplitudes of the AF signal.

HARDWARE SPECIFICATIONS

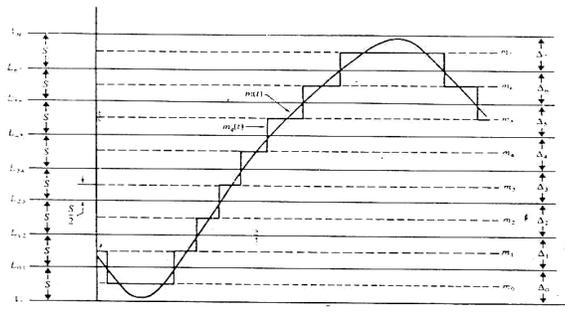
1. Analog Signal Sampling and Reconstruction Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 565 , 74163 , 555 , 8038 , CD 4053 , CA 3140.
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.



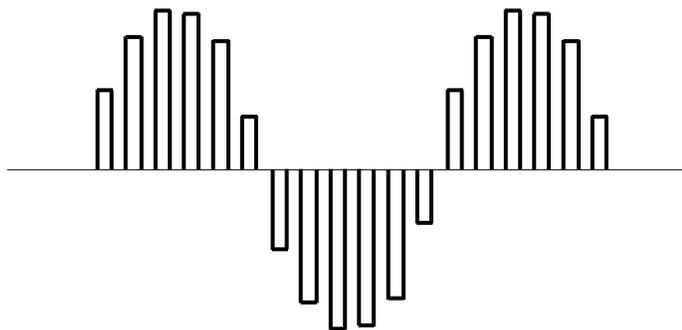
Modulating Signal Input



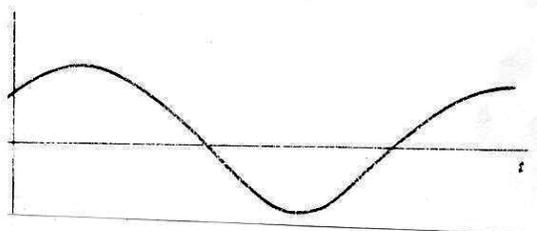
Sampling Input



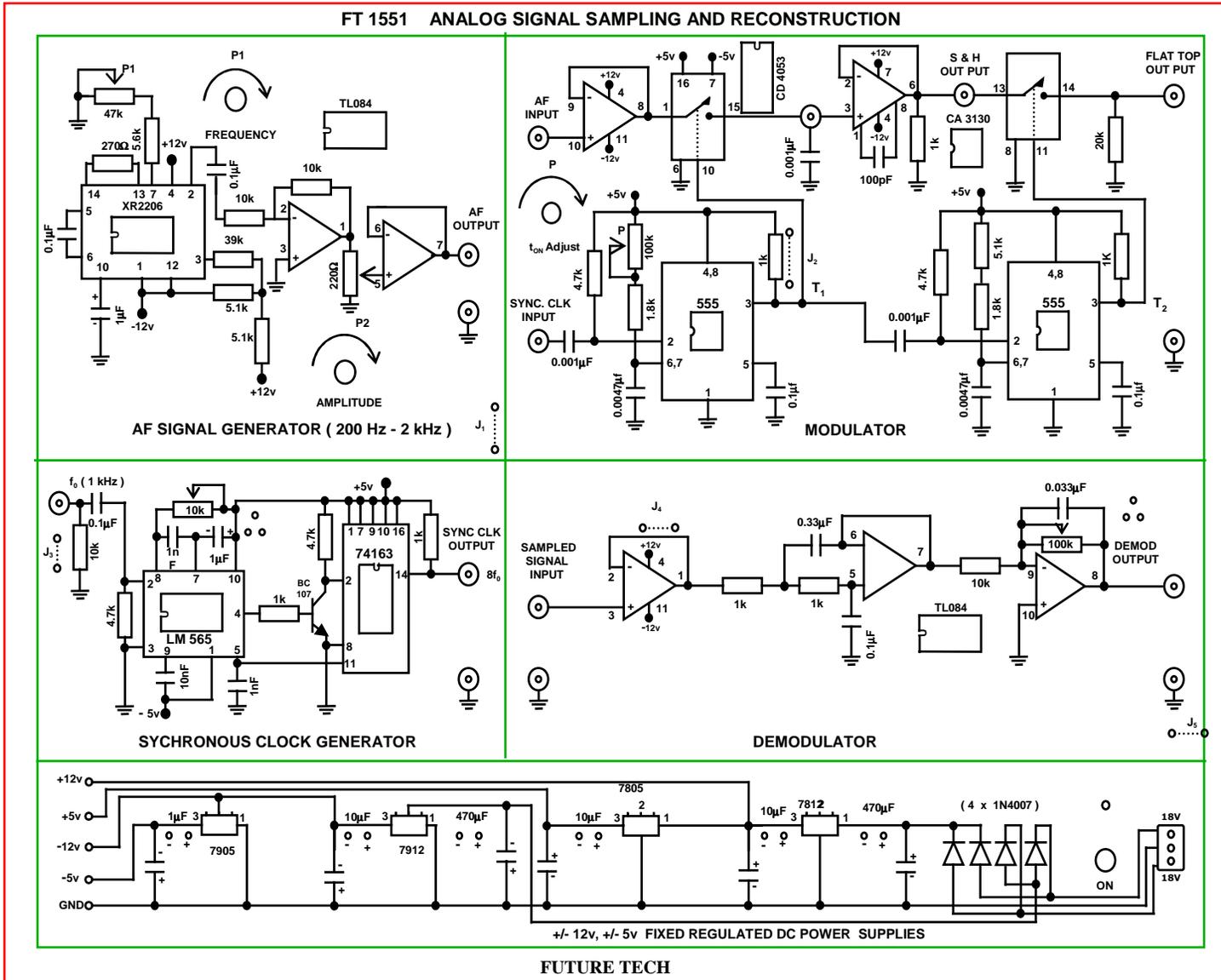
Sample and Hold Output



FLAT - TOP OUTPUT



DEMOMULTAED OUTPUT



PANEL LAYOUT DIAGRAM

PULSE AMPLITUDE MODULATION & DEMODULATION

AIM

To study Pulse Amplitude Modulation & Demodulation Process.

INTRODUCTION

Pulse Modulation is used to transmit analog information, such as speech signal. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only as pulse amplitude, together with any synchronising pulses that may be required. At the receiving end, the original waveform is reconstructed from the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation or Frequency Modulation, the resulting receiver output can have good reproduction with negligible or moderate distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be infinitely variable, while in the latter a code which indicates the sample Amplitude to the nearest predetermined level is sent. Pulse Amplitude Modulation is an analog communication which is discussed in the following section.

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz (Frequency and Amplitude variable)
2. Synchronous Clock Generator 8 kHz output and 1KHz input.
3. PAM Modulator
 - a) Natural Sampling
 - b) Sample and Hold
 - c) Flat - Top Sampling
4. PAM Demodulator consisting of
Low Pass Filter (3.4 kHz cut off) and Amplifier.
5. Built-in power supplies $\pm 12V/350$ mA, $\pm 5V/350$ mA.

CIRCUIT DESCRIPTION

1. AF SIGNAL GENERATOR

The AF Signal Generator designed around the popular Function Generator IC 8038 . The required range 200 Hz to 2 kHz is covered in a single range with one capacitor at pin 10. The Sine wave output is available at Pin 2, its symmetry is adjusted by a preset Pot of 10k, while the frequency is set by the P_1 Potentiometer 100k. Two amplifiers with +1 and $\cong -2$ gain in cascade act as buffers designed around TL084. The output amplitude is settable by the 1k Pot P_2 .

2. 8 KHz SYNCHRONOUS CLOCK GENERATOR

This is designed around a PLL IC 565 and a Binary Counter 74163. In order to enable the viewing of the PAM Pulse stably on Oscilloscope with respect to the analog signal, a high frequency clock (8 times the AF signal frequency) is generated using a VCO which is tuned to 16 kHz using a 100k pot provided between pins 8 and 10 of IC 565. When no signal is fed to the VCO, a chain of four FFs divides the 16 kHz to give 1 kHz output, which is fed back to the phase detector input at Pin 5 of 565.

The first Flip Flop output at Pin 14 yields 8 kHz frequency which is synchronous to the 1 kHz AF input. This is used as Sync. Clock in both modulator and demodulator.

3. PAM MODULATOR

The PAM modulator is designed around two Analog Switches (CD 4051) and Monostable Multivibrators using 555 ICs. A provision is made to observe Natural Sampling , Sample and Hold and Flat – Top Sampling of the PAM Signals.

The AF input is given to a unity gain buffer amplifier connected to an Analog Sampling Gate. The gate is controlled by switching pulses from a Monostable Multivibrator (555 IC) whose pulse width is set by potentiometer P. The Synchronous Clock provides the trigger pulses. The Monostable Multivibrator generates narrow pulses at the negative edge of the Synchronous Clock.

a) NATURAL SAMPLING : The switch in ' Natural Sampling Mode ' connects a 100K resistance to the output of the Sampling gate. In this mode the output is a PAM in which, during the Sampling width , the input signal is tracked. This is known as Natural Sampling. The output is given directly to the Demodulator to regenerate the AF signal. The effect of pulse width on its Demodulated output can be studied the maximum pulse width should be less than 50% of the input clock period.

b) SAMPLE AND HOLD : When the switch is kept in the ' Sample and Hold mode' , the input signal is tracked during the pulse width and held at the last level till the next pulse . In this mode the pulse width is adjusted to minimum . Instantaneous Sampling and Hold functions are activated. The S and H output can be Demodulated to get back the AF signal.

c) FLAT TOP SAMPLING : The Sample and Hold signal is again sampled after the sample . That is why the first Monostable pulses trigger second Monostable (555 IC) which has a fixed pulse width.

The second buffered Sampling gate is Sampled by the pulses which are generated after the first sample period is in the hold period irrespective of the pulse width . Therefore the output of the second sampling gate is always a Flat Top sample. This is another form of PAM which can be Demodulated using a filter and amplifier.

4. PAM DEMODULATOR

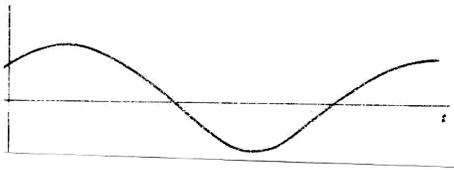
The PAM Demodulator consists of a Allen Sally second order Active Low Pass Filter preceded by a unity gain buffer and followed by a pre settable gain amplifier (TL 084.)

EXPERIMENTAL PROCEDURE

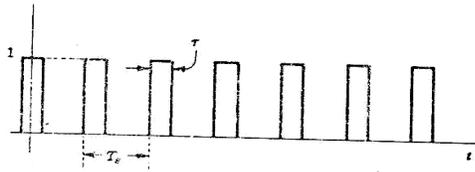
1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Observe the AF signal generator output in an Oscilloscope, it is a sinewave of frequency varying from 200 Hz to 2 kHz with 0-5V p-p Amplitude variation. Adjust the frequency to nearly 1 kHz, with the help of Potentiometer P_1 .
3. Observe the output of the 8 kHz Sync. Clock generator. Its frequency can be varied using 100k trim Pot. Adjust its free running frequency such that sync. Clock output is at 8 kHz
4. Connect the output of the AF signal generator to the 'Sync. Signal input' of the Sync. Clock generator shown at dashed line. Observe that both the signals are synchronised on the Oscilloscope. For this purpose feed the AF signal to CH1 of the Oscilloscope and the sync. Clock output to Ch 2 of the Oscilloscope. Select the trigger source as CH.1 and observe that both the signals are locked. Otherwise slowly adjust the AF signal frequency on either side of 1 kHz to get the frequency lock.
5. Connect the 'AF output' of AF signal generator to the 'AF input' of the PAM Modulator.
6. Connect the AF signal input to CH1 and Synchronous Clock to CH2 of the Oscilloscope. Choose the trigger to CH1. Both the signals will appear Synchronised.
7. Keep the switch in 'Natural Sampling' mode. Connect the CH 2 of the Oscilloscope to observe the Sampled output.
8. Now observe PAM pulses with Natural Top Sampling i.e., the top of the pulses will follow the input signal during the sampling period. This output can be given to Demodulator and the Demodulated output can be seen as replica of the AF output.
9. The effect of variation in AF frequency and amplitude can be studied at the output.
10. Alternately, the frequency and amplitude of the AF signal is brought back to 1kHz. Now the switch is kept in Sample and Hold mode.
11. The sampled output will appear a Stepped sine wave whose amplitude is held constant for the rest of the period after the sampling pulse.
12. This is also a form of PAM which can be Demodulated and seen at the Demod output.
13. Now connect the CH2 of the oscilloscope to Flat Top output. We observe Flat Top PAM pulses which are present in the post sampling period.
14. Connect these pulses to the Demodulator and observe the Demod output.
15. Thus the trainer is useful in observing natural Sampled PAM pulses, S&H PAM pulses and Flat Top PAM pulses at different frequencies and amplitudes of the AF signal.

HARDWARE SPECIFICATIONS

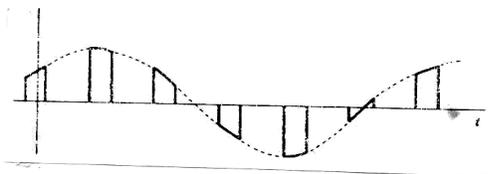
1. Pulse Amplitude Modulation and Demodulation Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 565, 74163, 555, 8038, CD 4053, CA 3140.
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.



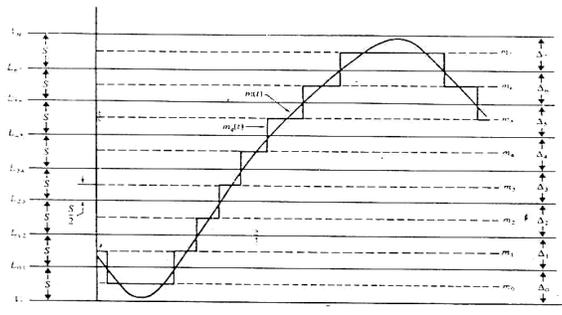
Modulating Signal Input



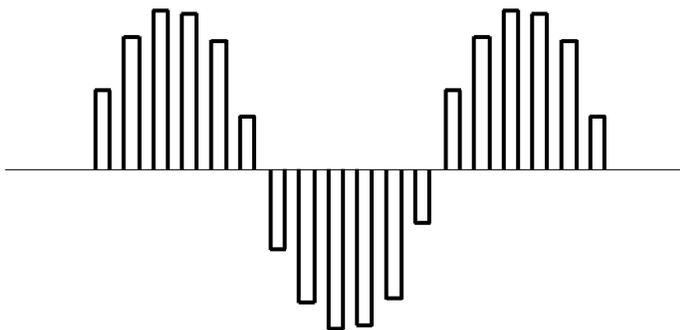
Sampling Input



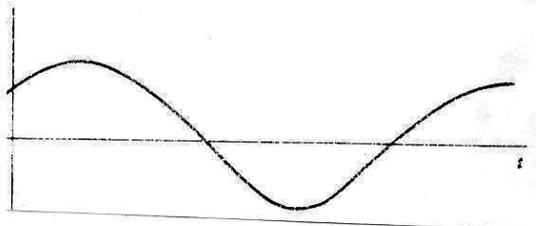
Natural Top Sampling Output



Sample and Hold Output

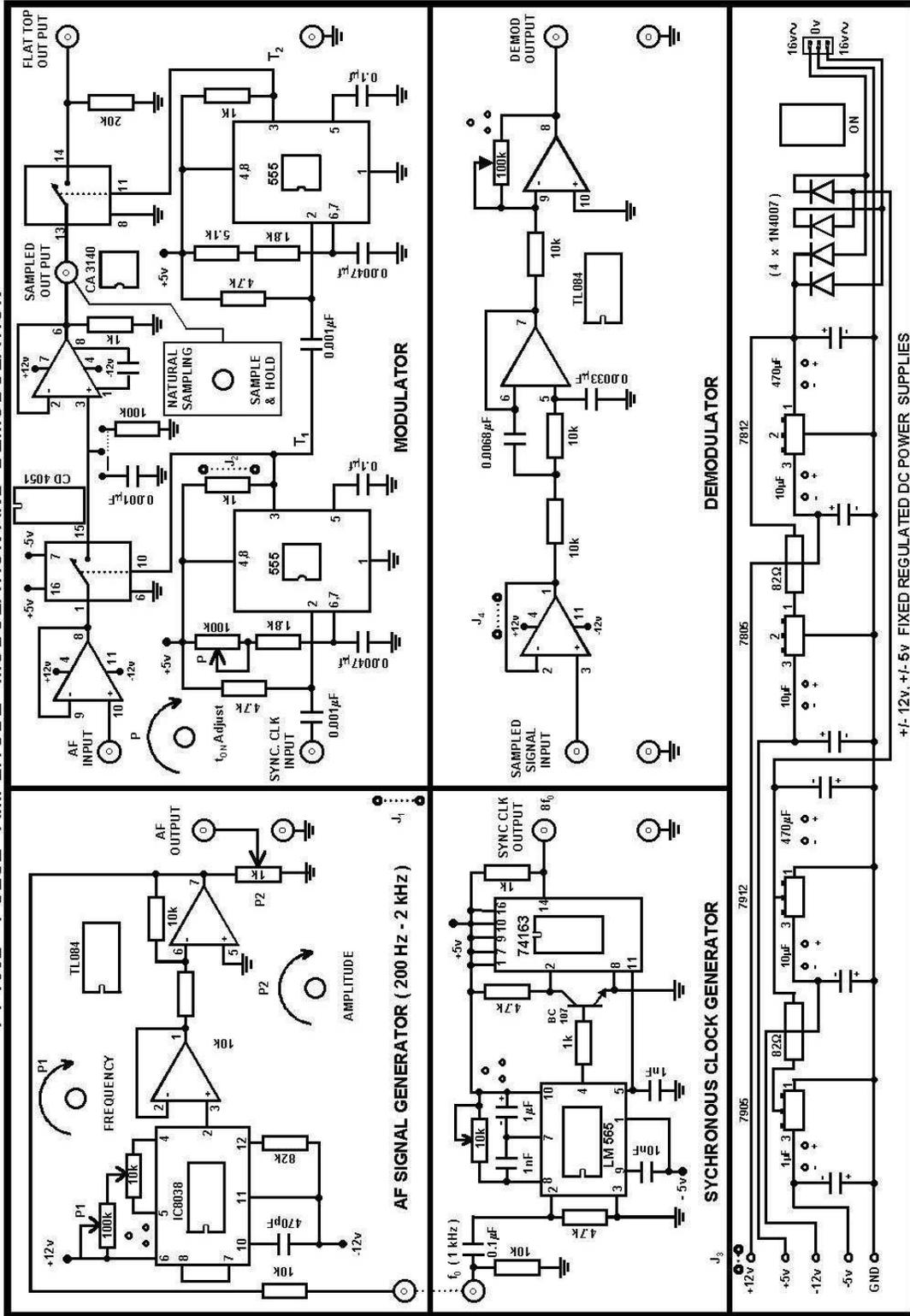


FLAT - TOP OUTPUT



DEMOMULTAED OUTPUT

FT 1552 PULSE AMPLITUDE MODULATION AND DEMODULATION



FUTURE TECH

PANEL DIAGRAM

PULSE WIDTH MODULATION & DEMODULATION

AIM

To study Pulse Width Modulation & Demodulation Process.

INTRODUCTION

Pulse Modulation is used to transmit analog information, such as speech signal. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only as pulse width together with any synchronising pulses that may be required. At the receiving end, the original waveform is reconstructed from the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation or Frequency Modulation, the resulting receiver output can have good reproduction with negligible or moderate distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Width may be continually variable, while in the latter a code which indicates the sample Amplitude to the nearest predetermined level is sent. Pulse Width Modulation is an analog communication which is discussed in the following section.

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz (Frequency and Amplitude variable)
2. Synchronous Clock Generator 8 kHz output and 1KHz input.
3. PWM Modulator
4. PWM Demodulator consisting of
Low Pass Filter (3.4 kHz cut off) and Amplifier.
5. Built-in power supplies $\pm 12V/350$ mA, $\pm 5V/350$ mA.

CIRCUIT DESCRIPTION

1. AF SIGNAL GENERATOR

The AF Signal Generator is designed around the popular Function Generator IC 8038 . The required range 200 Hz to 2 kHz is covered in a single range with one capacitor at pin 10. The Sine wave output is available at Pin 2, its symmetry is adjusted by a preset Pot of 10k, while the frequency is set by the P_1 Potentiometer 100k. Two amplifiers with +1 and $\cong -2$ gain in cascaded act as buffers designed around TL084. The output amplitude is settable by the 1k Pot P_2 .

2. 8 KHz SYNCHRONOUS CLOCK GENERATOR

This is designed around a PLL IC 565 and a Binary Counter 74163. In order to enable the viewing of the PWM Pulse stably in an Oscilloscope with respect to the analog signal, a high frequency clock (8 times the AF signal frequency) is generated using a VCO which is tuned to 16 kHz using a 100k pot provided between pins 8 and 10 of IC 565. A chain of four FFs divides the 16 kHz to give 1 kHz output, which is fed back to the phase detector input at Pin 5 of 565.

The first Flip Flop output at Pin 14 yields 8 kHz frequency which is synchronous to the 1 kHz AF input and this Sync Signal is connected as shown in dashed lines. This is used as Sync. Clock in both modulator and demodulator.

3. PWM MODULATOR

PWM modulator consists of one stage of resettable Monostable Multivibrator 555 IC.

The Sync. Clock is given at the Trigger input (Pin 2) and the AF input is given at (Pin 5.) which is the control voltage input of the 555 IC.

The 555 IC is triggered at the -Ve edge of the Clock . The pulse is reset depending upon the amplitude of the analog input at pin 5 thus generating PWM pulses. The output pulses at pin 3 are positive pulses with the rising edge at fixed time position (that is the falling edge of the sync. Clock), while the falling edge of the output is time modulated with respect to the analog input . This is PWM Pulse Stream .

4. PWM DEMODULATOR

The PWM Demodulator consists of an Allen Solly second order active Low Pass Filter preceded by a unity gain buffer and followed by a pre settable gain amplifier (TL 084.)

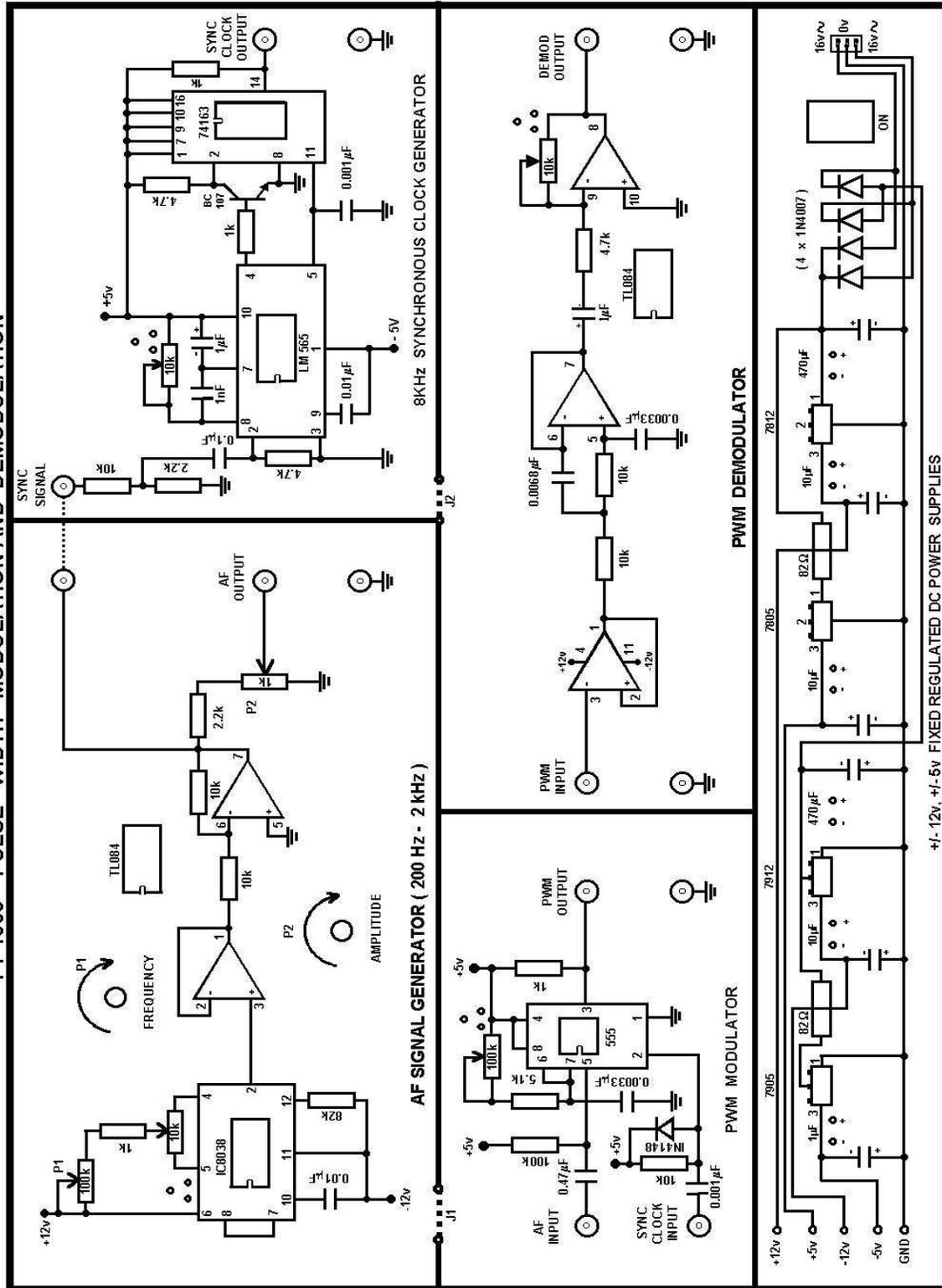
EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Observe the 'AF output' in an Oscilloscope, it is a sinewave of frequency varying from 200 Hz to 2 kHz with 0-5V p-p Amplitude variation. Adjust the frequency to nearly 1 KHz, with the help of Potentiometer P_1 .
3. Observe the output of the 8 kHz Sync. Clock generator. Its frequency can be varied using 100k trim Pot. Adjust its free running frequency such that sync. Clock output is at 8 kHz
4. Connect the output of the AF signal generator to the 'Sync. Signal input' of the Sync. Clock generator shown at dashed line. Observe that both the signals are synchronised on the Oscilloscope. For this purpose feed the AF signal to Ch.1 of the Oscilloscope and the sync. Clock output to Ch 2 of the Oscilloscope select the trigger source as CH.1 and observe that both the signals are locked. Otherwise slowly adjust the AF signal frequency on either side of 1 kHz to get the frequency lock.
5. Connect the 'AF output' of AF signal generator to the 'AF input' of the PWM Modulator. Connect the 'Sync Clock' output to the 'Sync Clock' input of the PWM Modulator
6. Connect the AF signal input in CH1 and Synchronous Clock in CH2 of the Oscilloscope. Choose the trigger to CH1. Both the signals will appear Synchronised.
7. Observe the 'Sync clock input' on CH1 and 'PWM output' on CH2 of the oscilloscope select the trigger source to CH1 and trigger edge to -Ve.
8. When the AF signal amplitude is Zero the PWM Pulses are observed as varying positive pulses. All the pulses start at the negative edge of the clock and end as per the instantaneous amplitudes of AF signal.
9. Now increase the amplitude of the AF signal, the pulse width varies on right side of the rising edge marked at reference. The variation in time corresponds to the amplitudes of the input at that instant. Measure the amplitude and time Variation which gives a correspondence of $\mu\text{s} / \text{v}$ modulation quotient.
10. Connect the 'PWM output' of the Modulator to 'PWM input' of the demodulator. Observe the Demodulated output, which is same as the input.
11. Connect the AF output on CH 1 and Demodulated output on CH2. Vary the AF output amplitude and observe the corresponding variation in the output of the demodulator.

HARDWARE SPECIFICATIONS

1. Pulse Width Modulation and Demodulation Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 565, 74163, 555, 8038, CA 3140.
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.

FT 1553 PULSE WIDTH MODULATION AND DEMODULATION



FUTURE TECH

PANEL DIAGRAM

PULSE POSITION MODULATION & DEMODULATION

AIM

1. To study the generation of PPM signal and its Demodulation .
2. To study the effect of Amplitude & Frequency of the Modulating signal on its output
3. To study the effect of the Frequency of sampling signal on the Demodulated output.

INTRODUCTION

Pulse Modulation is used to transmit analog information, such as speech signal. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only as pulse amplitude, pulse width or pulse position, together with any synchronising pulses that may be required. At the receiving end, the original waveform is reconstructed from the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation or Frequency Modulation, the resulting receiver output can have moderate distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be infinitely variable, while in the latter a code which indicates the sample Amplitude to the nearest predetermined level is sent. Pulse Position Modulation is an analog communication which is discussed in the following section.

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz.
2. Synchronous clock Generator 8 kHz.
3. PPM Modulator based on 555 Timer Ics.
4. Demodulator consisting of PPM to PWM Comparator and Active Low Pass Filter (3.4 kHz cut off).
5. Built-in power supplies $\pm 12V/350$ mA, $\pm 5V/350$ mA.

CIRCUIT DESCRIPTION

1. AF SIGNAL GENERATOR

The AF Signal Generator designed around the popular Function Generator IC 8038 . The required range 200 Hz to 2 kHz is covered in a single range with one capacitor at pin 10. The Sine wave output is available at Pin 2, its symmetry is adjusted by a preset Pot of 10k, while the frequency is set by the P_1 Pot 100k. Two amplifiers with +1 and $\cong -2$ gain in cascaded act as buffers designed around TL084. The output amplitude is settable by the 1k Pot P_2 .

2. 8 KHz SYNCHRONOUS CLOCK GENERATOR

This is designed around a PLL IC 565 and a Binary Counter 74163. In order to enable the viewing of the PPM Pulse stably with respect to the analog signal, a high frequency clock (8 times the AF signal frequency) is generated using a VCO which is tuned to 16 kHz using a 100k pot provided between pins 8 and 10 of IC 565. When no signal is fed to the VCO, a chain of four FFs divides the 16 kHz to give 1 kHz output, which is fed back to the phase detector input at Pin 5 of 565.

The first Flip Flop output at Pin 14 yields 8 kHz frequency which is synchronous to the 1 kHz AF input. This is used as Sync. Clock in both modulator and demodulator.

3. PPM MODULATOR

PPM modulator consists of two stages. The first stage generates PWM Pulses while the second stage generates PPM pulses from PWM pulses both using 555 Timer ICs.

The Sync. Clock is given at the Trigger input (Pin 2) and the AF input is given at (Pin 5.) which is the control voltage input of the 1st 555 IC.

The 555 IC is triggered at the -Ve edge of the Clock . The pulse is reset depending up on the amplitude of the analog input at pin 5 thus generating PWM pulses. The output at pin 3 are positive pulses with the rising edge at fixed timer position (that is the falling edge of the sync. Clock). While the falling edge is time modulated with respect to the analog input . This is PWM Pulse Stream .

The second 555 Timer generates fixed narrow pulses at the trailing edge of the PWM pulses. Their position varies in time with respect to the negative edge of the clock. This is PPM Pulse Stream.

4. PPM DEMODULATOR

The PPM output is reconverted into PWM output by giving it to the Set and Reset inputs of a Flip-Flop constructed by four Nand gates, in which one input is the PPM Signal while the other input is the Synchronizing clock. The PWM output is passed through a low pass Filter (3.4 kHz cut off) to regenerate the Modulating AF signal.

EQUIPMENT REQUIRED

1. Pulse Position Modulation and Demodulation Trainer.
2. Oscilloscope - 20 MHz, Dual Trace.
3. Patch chords (1set) and User Manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Observe the AF signal generator output in an Oscilloscope, it is a sinewave of frequency varying from 200 Hz to 2 kHz with 0-5V p-p Amplitude variation. Adjust the frequency to nearly 1 KHz, with the help of Potentiometer P_1 .
3. Observe the output of the 8 kHz Sync. Clock generator. Its frequency can be varied using 100k trim Pot. Adjust its free running frequency such that sync. Clock output is at 8 kHz
4. Connect the output of the AF signal generator to the 'Sync. Signal input' of the Sync. Clock generator shown at dashed line. Observe that both the signals are synchronised on the Oscilloscope. For this purpose feed the AF signal to Ch.1 of the Oscilloscope and the sync. Clock output to Ch 2 of the Oscilloscope select the trigger source as ch.1 and observe that both the signals are locked. Otherwise slowly adjust the AF signal frequency on either side of 1 kHz to get the frequency lock.
5. Connect the 'AF output' of AF signal generator to the 'AF input' of the PPM Modulator.
6. Connect the 'Sync. Clock output' to the 'Sync. Clock input' of the PPM Modulator.
7. Observe the 'Sync clock input' on Ch 1 and 'PPM output' on ch2 of the oscilloscope select the trigger source to ch1 and trigger edge to -Ve.
8. When the AF signal amplitude is Zero the PPM Pulses are observed as narrow pulses spaced equidistant and at constant time delay with respect to the -ve edge of the clock. Mark this as reference position.
9. Now increase the amplitude of the AF signal, the pulse position varies on either side of the reference position marked at reference earlier. The total variation in time corresponds to the peak to peak amplitudes of the input. Measure the Peak to Peak amplitude and Peak to Peak time Variation which gives a correspondence of $\mu s / v$ modulation quotient.
10. Alternately observe the sinewave (1 kHz gives to Sync.Clock) on ch1. and PPM output on Ch2. of the oscilloscope. Select Ch 1 as trigger source.
11. Adjust the AF amplitude to Zero using pot P1.
Using the uncalibrated knob of the oscilloscope adjust the wave form such that each pulse is at the beginning of each division (big) of the scope time scale. This is done so as to make the further measurements easy.
At this stage each division is equal to T mSecs (the time period of the Sync. clock.)
There are now 10 pulses on the screen and just more than 1 cycle of the sinewave.

12 Now increase the amplitude of the sinewave to Max. Connect the Ch1 of the oscilloscope to AF input now.

Note the displacement of each of the pulses on ch2 from the original position and the corresponding amplitude of AF signal at the beginning of the division . Compute $\mu s / v$ at each point and its average value which gives the modulation quotient.

13 Connect the 'PPM output' of the Modulation to 'PPM input' of the demodulator.

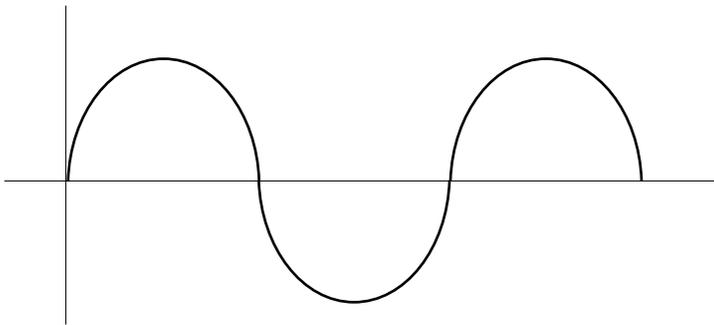
Also connect the sync. Clock input to the demodulator. Observe the demodulated output, which is same as the input.

Connect the AF output on Ch. 1 and Demodulated output on Ch.2

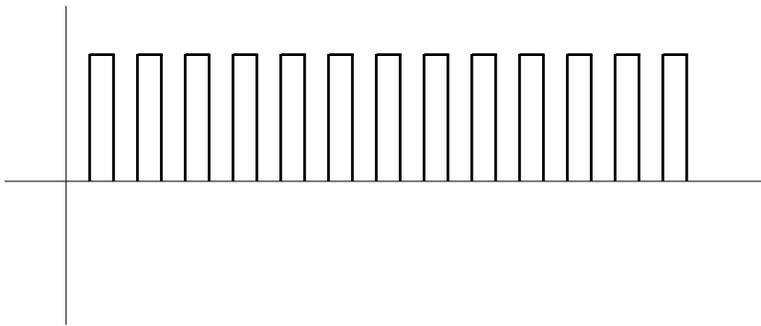
Vary the AF output amplitude and observe the corresponding output of the demodulator.

14 The Sync. Clock generator will not synchronise for all the range of frequencies of the AF Signal Generator.

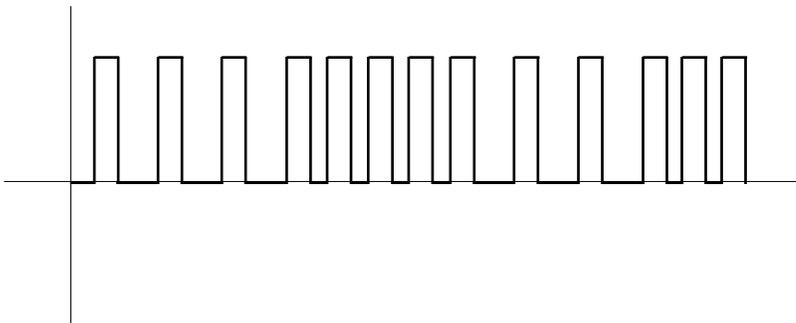
However the Sync signal input may be disconnected and the AF input output can be studied for all AF signal . Observation of PPM pulses stably on the scope will be difficult for measurement purposes in this condition.



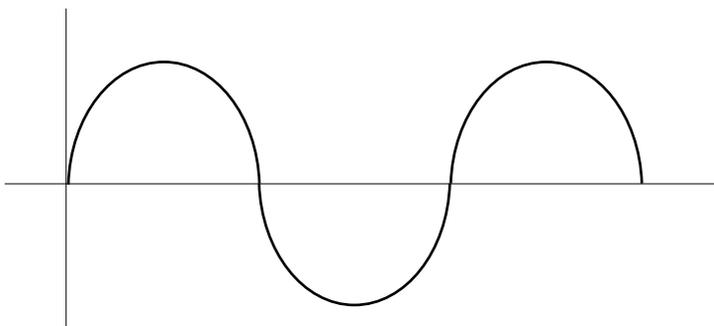
AF SIGNAL



**SYNCHRONOUS
CLOCK**



**PPM MODULATED
OUTPUT**



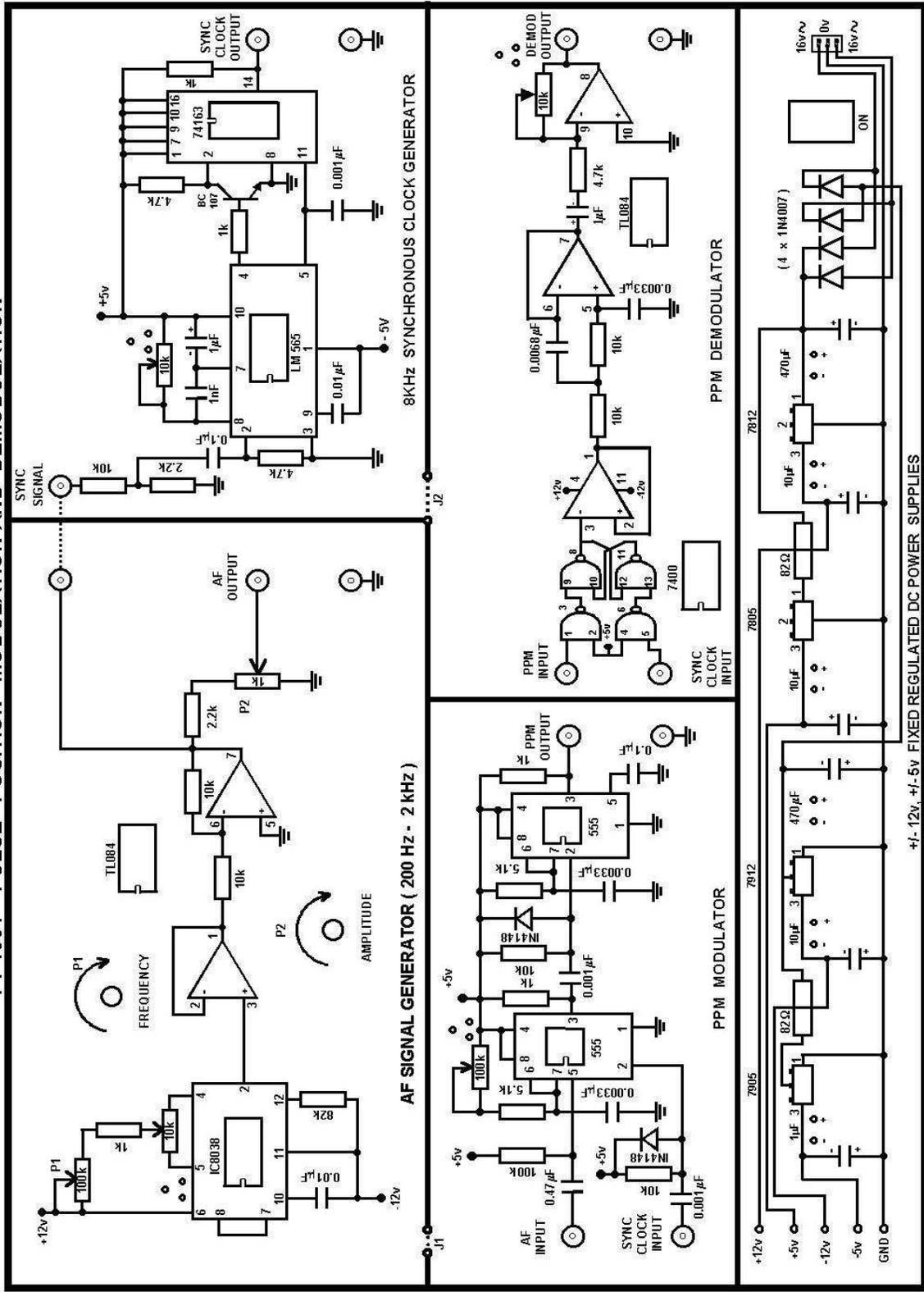
**DEMODULATED
OUTPUT**

WAVE FORMS FOR PPM MODULATION AND DEMODULATION

HARDWARE SPECIFICATIONS

1. Pulse Position Modulation and Demodulation Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 565 , 74163 , 555 , 8038 , 7400 .
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.

FT 1554 PULSE POSITION MODULATION AND DEMODULATION



FUTURE TECH

PANEL LAYOUT DIAGRAM

ANALOG TIME DIVISION MULTIPLEXING & DEMULTIPLEXING

AIM

1. To study the 4 Channel Analog Multiplexing and Demultiplexing
2. To study the Adjacent channel cross take.
3. To study the effect of Sampling frequency on output signal characterized
4. To study the effect of input signal amplitude on the output signal characteristics.

INTRODUCTION & THEORY

Only one Analog Base Band signal can be transmitted over a single channel without the use of any modulation techniques. However, amplitude modulation by different carriers like in (FDM), one could multiplex and transmit various analog signals on the same channel at the same time. Besides, the Space Diversity and Frequency Diversity, there is yet another method of sending multiple analog signals on a single channel using Time Division Multiplexing (TDM) technique.

HARDWARE SPECIFICATIONS

- 1 Quad signal sources
 - a) Sine wave
 - b) Square wave
 - c) Triangular wave all the three at the same variable frequency
 - d) Sine wave at fixed different frequency
- 2 4 Channel Multiplexer
- 3 4 Channel Demultiplexer
- 4 Low Pass Filter & Amplifier
- 5 Built in Power Supplies $\pm 12v, \pm 5v$ @350mA each.

CIRCUIT DESCRIPTION

1 QUAD SIGNAL SOURCES

The 8038 is a versatile Function Generator IC which generates Sine, Square and Triangle waveforms. The frequency range of 200 Hz to 2 kHz is generated. The Sine wave Symmetry is adjustable by means of a preset 10k Ω Potentiometer. The 100K potentiometer adjusts the frequency of Oscillations. The Sine wave output of 8038 at Pin 2 is buffered by an OP Amps TL084. The final output attenuated and is fed through a 1k Ω Potentiometer to adjust to required amplitude.

The Triangular wave form is generated at Pin 3 of 8038 IC . An OP Amp is used as buffer . The output of the buffer is attenuated and is fed through a 1k Pot for continuous amplitude control.

The Square form is generated at Pin 9 of 8036 IC . An Op Amp is used as a buffer . The output of the buffer is attenuated and is fed through a 1k Pot for continuous amplitude control.

2 FIXED FREQUENCY SINE WAVE GENERATOR

The Sine wave is generated using two Op Amps of the type TL084. The two Op Amps are configured in Integrator mode such that the first Op Amp produces 180° Phase Shift while the second one produces a further 180° Phase Shift. The output of second Op Amp is limited by a back to back series connected Zener diodes (5.1 V each). The circuit generates a Fixed Sine wave frequency of 1KHz, which is one of the test signal, for the multiplexer input.

3 4 CHANNEL MULTIPLEXER

CD 4052 is a 4 Channel Analog Multiplexer which can accept analog signal in the range from 0 to $\pm 2.5 V_p$. The channel selection is done by the signals A_1 & B_1 ($+2$ & $+4$ outputs of FF). A 2 to 4 Decoder built in CD4052 decodes these two signals and controls the 4 position analog switch. The common output (TDM analog output) is available at Pin 3. A 555 Timer in Astable mode with frequency control pot generates square waves which clocks the first Flip Flop. The output of first Flip Flop clocks the second one.

4 4 CHANNEL DEMULTIPLEXER

The Multiplexed PAM signal is given to the 4 Channel Demultiplexer input at Pin 13. The A_1 & B_1 timing wave forms selects the channel and accordingly connects the same to the output. Thus at the output the PAM signals of each channel are separated.

5 LOW PASS FILTER & AMPLIFIER

The PAM signal from any one channel can be connected to the Low Pass Filter (3.4 kHz cut of frequency) preceded by a unity gain buffer, which gives the analog output. This being at low level an amplification with adjustable gain is used to amplify the signal. The LP Filter output when connected to the amplifier gives a boosted output which is a replica of input. Thus any one selected channel can be seen at the output of the Amplifier.

EXPERIMENTAL PROCEDURE

There are 4 signal sources; viz;

- a. **Sine wave signal** at Socket 1.
- b. **Triangular wave signal** at Socket 2.
- c. **Square wave signal** at Socket 3.
- d. Another **Sine wave signal** at socket 4.

1a. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.

1b. Connect these four signals to four inputs of the Multiplexer, Adjust each signal amplitude to be within $\pm 2V_{p-p}$ and frequency non overlapping, Within a frequency band of 2kHz.

2 Adjust the frequency of 555 Timer to be around 32 kHz, so that each of the 4 channels is sampled at 8kHz.

3 Observe $+4$ output Pin 11 of 7476 on one channel 1 and TDM output Pin 13 of CD4052 on second channel of Oscilloscope select trigger source as CH1. All the multiplexed channels are observed during the full period of the clock ($1/32$ kHz) 31.25 μ Sec

4 Connect the TDM output pulses to TDM input of Demultiplexer at Pin 13 of CD4052. Observe the individual outputs 1,2,3,4 at Pin 12,14,15,11 of CD4052 respectively. The TDM pulses corresponding to each channel are now separated as 4 streams.

- 5 Take any output of the Demodulator and connect it to Filter and . Observe the output of the Amplifier in conjunction with the corresponding input. Repeat this for all 4 inputs. This is the Demodulated TDM output. Any slight variation in frequency or amplitude is reflected in the corresponding output .
- 6 Vary the frequency of Sampling by potentiometer P_1 connected to 555 and observe the effect on the individual outputs

II TO STUDY THE ADJACENT CHANNEL CROSS TABLE

- 1 Keep the input signal at CH1 of Multiplexer and restore its Amplitude & Frequency to original settings. Ground the rest of the other three inputs.
- 2 Connect the CH1 output of Demultiplexer to Low Pass Filter and Amplifier chain .
- 3 Measure its amplitude V_{PP1} on the Oscilloscope for CH1 output.
- 4 Now connect CH 4 output of Demodulator to Filter and Amplifier. Measure the output V_{PP4} . (this is one of the adjacent channel to CH 1).
- 5 Connect CH 2 output to Filter & Amplifier. Measure the output – V_{PP2}

$$6 \text{ Compute } 20 \log \frac{V_{PP4}}{V_{PP1}} \quad \& \quad 20 \log \frac{V_{PP2}}{V_{PP1}}$$

This will give the adjacent channel cross talk in dB. It should be better than 40 dB.

III EFFECT OF SAMPLING FREQUENCY ON OUTPUT

- 1 Keep the setup as in the previous experiment (II) with CH1 input to Multiplexer.
- 2 Connect the CH1 output of Demultiplexer unit to Filter and Amplifier.
- 3 Vary the Sampling clock frequency of 555 from 32 kHz above and below.
- 4 Above 32 kHz, no perceptible difference is observed . Because the sampling frequency is much above Nyquist rate. When the frequency is decreased to below 8 kHz (i.e each channel Sampling frequency to 2 kHz for 1 kHz Analog signal) The signal distortion sets in deterioration of its shape starts . (Nyquist Theorem.)

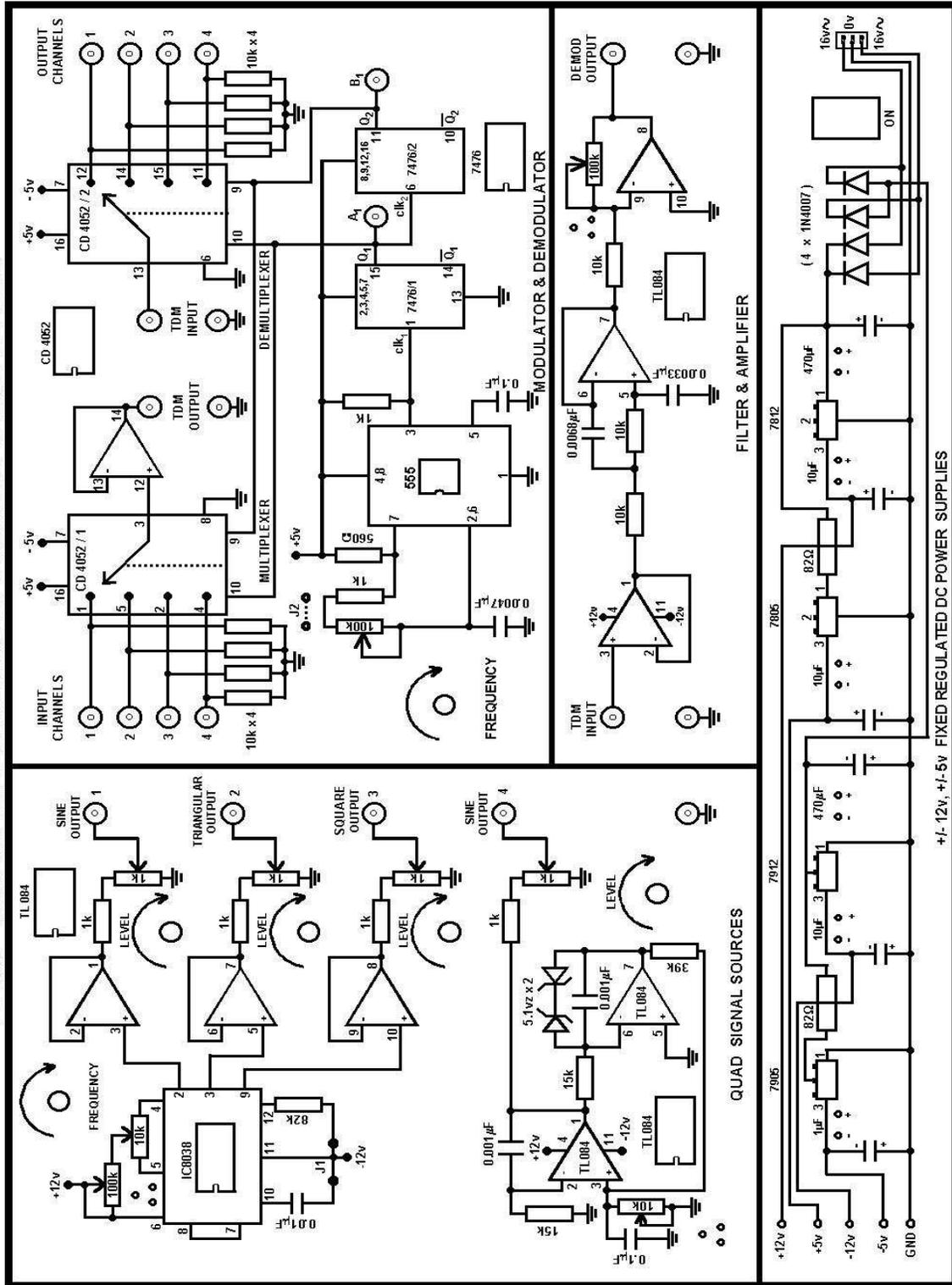
IV EFFECT OF AMPLITUDE ON THE OUTPUT.

- 1 Keep the same setup as in the previous experiment (ii) with CH1 input alone at 1kHz and $\pm 2V_{PP}$ amplitude.
- 2 Select the CH1 output of Demultiplexor and connect it to Filter and Amplifier.
- 3 Vary the Amplitude of the Input above $2.5 V_{PP}$ Sine wave gets clamped due to the Multiplexer input limitations.
- 4 At very low amplitude levels the Signal to Noise ratio will be poor.

HARDWARE SPECIFICATIONS

1. Analog Time Division Multiplexing and Demultiplexing Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 555 , 8038 , CD 4052 , 7476 .
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.

FT 1557 ANALOG TIME DIVISION MULTIPLEXING AND DEMULTIPLEXING



FUTURE TECH

PANEL LAYOUT DIAGRAM

PULSE CODE MODULATION & DEMODULATION

AIM

1. To Study the Pulse Code Modulation and Demodulation.
2. To Study the effect on the variation of the Amplitude of the Modulating Signal.
3. To Study the variation of Sampling frequency on the output Demodulation signal and to prove the Nyquist Sampling Theorem.

INTRODUCTION & THEORY

In analog communication systems, the limitation is that once noise is introduced at any place along the channel, we are 'stuck up' with it. To overcome such a situation, a process known as 'Quantisation' is introduced in which the analog signal is approximated to the nearest whole number of small steps of each size S . This process of quantisation is during every sampling interval. Sampling of the Analog signal however is done at a rate keeping in view of the Nyquist criterion.

In the process of quantisation approximation is made to make the number of steps a whole number resulting in an approximation error of $\pm S/2$. This approximation noise or quantisation noise is reproduced in the demodulation and is inseparable from the original signal.

The quantised steps represented as a binary number (of Pulses) is transmitted to the Receiver. This whole process of sampling, Quantisation and conversion into a Binary code is known as Pulse Code Modulation (PCM). Thus in PCM the code represented at a particular time slot (sampling period) is representative of the instantaneous amplitude of the Analog signal.

At the receiving end, the pulses which are accompanied by noise or rounded off due to channel bandwidth limitation are reconstructed and clock frequency is derived from it using PLL techniques. The reconstructed signal retimed with the regenerated clock.

The resulting digital signal is converted into Analog form using D/A Converter and Low Pass Filter.

The PCM signal being in digital from transmission through low quality channels (with low SNR is possible without any loss of quality).

However the band width required for PCM signals increases largely on the basis of Sampling frequency and number of clock pulses per sample.

The Digital Telephony, Digital Video etc. are a result of PCM techniques being used extensively for better quality in combating noise in transmission.

HARDWARE DESCRIPTION :

SIGNAL SOURCES

1. AF Signal Generator : 200Hz - 2KHz
2. Clock Generator
 - Conversion Clock : 68KHz - 300 KHz
 - Data Clock : 32KHz - 150 KHz
 - Byte Clock : Data Clock
 - Sampling Clock : 8.75KHz - 19KHz
3. Variable DC Source : +2.5V - -2.5V

PCM MODULATOR

4. Analog Sample and Hold.
5. 8 Bit Analog to Digital converter.
6. Parallel to Serial converter.

PCM DEMODULATOR

7. Serial to Parallel converter.
8. 8 Bit Latch.
9. 8 Bit Digital to Analog converter with Current output.
10. Current to Voltage converter
11. Low Pass Filter(3.4KHz cut off).

CIRCUIT DESCRIPTION :

1. AF SIGNAL GENERATOR

The 8038 IC is a versatile Function Generator IC which generates Sine ,Square and Triangle Waveforms. The frequency is 200Hz to 2KHz which is generated by an independent capacitor 0.01 μ F. The Sine wave Symmetry is adjustable by means of a preset 10K Ω connected between pins 4 and 5 of the IC 8038. The 100K Ω potentiometer adjusts the frequency of oscillations . The Sine wave output of 8038 at pin 2 is buffered by two Op Amps of TL084. The first Op Amp gives a unity non inverting gain while the latter gives an inverting gain of unity. The final output is taken through a 1K Ω potentiometer to adjust to required amplitude.

Additionally a DC signal variable from 0V to \pm 2.5V DC is provided through a potentiometer P₃ for studying steady-state conditions.

2. CLOCK GENERATOR

The circuit is designed around the popular timer IC 555 operated in Astable mode.Using a timing capacitor of 470pF and a potentiometer P₄ which is 22K Ω the required variation of 68KHz to 300KHz Square wave output is generated.

This output is divided by Flip - Flop in 74163 IC to give frequencies from 34Hz to 150KHz. This is used as a Bit clock in PCM.

3. SAMPLE PULSE GENERATOR

The output of Bit clock generator i.e 34KHz to 150KHz is given to a series of 3 Flip-Flops(divided by 8) to give frequencies from 8.75KHz to 19KHz.

4.ANALOG SAMPLE AND HOLD

The Analog Signal from the AF Signal Generator or Variable DC Source is buffered by a unity gain non inverting amplifier connected to the Sampling gate. The Buffer Amplifier is used to give a low output impedance so that the Hold capacitor gets charged instantaneously. CD4052 Analog Switch is used as a Sampling gate.

The gate is closed during the 'ON' time (+5V) of the Sampling Pulse and open (0V) during its 'OFF' time. During the 'OFF' time the capacitor holds the output level of the signal.

5. ANALOG TO DIGITAL CONVERTER

ADC 0800 is an 8 Bit Analog to Digital converter using successive approximation method. A high frequency Conversion Clock converts the Analog Signal into a Parallel Digital Word. For the Input range varies from -2.5V to +2.5V, the output varies monotonically from 00 to FF i.e -126 to +126 levels(i.e total 256 levels).

6. PARALLEL TO SERIAL CONVERTER

The Parallel Digital Word from the ADC is transferred by Parallel Load Clock in a Parallel to Serial Converter 74165. A Serial Shift Clock which is 8 times higher than Parallel Load Clock shifts the Bits in the 8 Bit Word serially. This is the Serial PCM Data.

7. SERIAL TO PARALLEL CONVERTER

At the Demodulating end the received Serial data is converted back into a Parallel Word using Serial to Parallel converter 74164. The same Serial Shift Clock helps in shifting the bits.

8. 8 BIT LATCH

The Parallel Word available at the Serial to Parallel Converter cited above is transferred into 8 Bit Word in a 8 Bit Latch (74374) using Parallel Load Clock. The 8Bit Word is held till the next word arrives after the next Sampling Pulse.

9. DIGITAL TO ANALOG CONVERTER

The DAC 0800 is a 8 Bit Digital to Analog Converter. The output is proportional (current form) to the Bit Code present at the 8 data input. An Op Amp is used to convert the output current to voltage. This output voltage is in the form of a stepped waveform similar to the S & H waveform except for the quantisation error.

10. LOW PASS FILTER

The stepped Analog waveform from the DAC is filtered and smoothed by a Low Pass Filter with 3.4KHz cut off frequency. This is a replica / reproduced / demodulated Analog Signal.xx

EQUIPMENT REQUIRED

1. FUTURE TECH Pulse Code Modulation and Demodulation Trainer.
2. Oscilloscope - 20 MHz , Dual Trace.
3. Set of Patch Chords (1set).
4. User Manual.

EXPERIMENTAL PROCEDURE

I. STUDY OF THE PULSE CODE MODULATION AND DEMODULATION

- 1a Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
- 1b Observe the 'Analog output' signal on the Oscilloscope .Familiarize its variation of amplitude and frequency by means of potentiometers P_1 and P_2 .
2. Set the frequency about 1KHz and its amplitude to $\pm 2.5V$ (i.e 5V p-p).
3. Connect the 'Analog output' to the ' Analog input 'of the Sample and Hold circuit using a 2mm patch chord.
4. Observe the output of 555 IC timer 'Conversion Clock output ' . Observe the variation of frequency by means of Potentiometer P_4
5. Simultaneously observe the ' Parallel Load Clock output ' (I.e divided by 16) on the other channel of the Oscilloscope
6. Adjust the frequency of 'Sampling Clock' so that its is about 8KHz and connect it to Sample and Hold circuit using a 2mm patch chord.
7. Observe the Analog output Signal and Sample and Hold output on both the channels of the Oscilloscope.
8. During the 'ON' period of Sampling Pulse the 'Analog Signal' is sampled and during its 'OFF' period the Analog Signal' value is held.Vary the Analog frequency on either side of the set value and observe the S&H output.
9. Connect S&H output to the ADC 'S&H input' and the 555 IC 'Conv Clock output' to ADC 'Conv Clock input'.
The ADC 0800 successive approximation 8 Bit Analog to Digital Converter. The 8 successive pulses convert the Analog input into 8 Bits which appear in Parallel format. This can be observed on the LEDs provided after the ADC.
10. Observe the PCM output (Serial Shift Data) on CH1 and Sample Clock on CH2 of the Oscilloscope.
11. The PCM Serial output is already connected internally to PCM Demodulator input.
12. The Serial Shift Clock and Parallel Load Clock to the Demodulator are also connected internally.
13. Observe the output of the DAC of the amplifier (used as I to V converter) at pin 1 of TL 084(D/A output) . The DAC output resembles the S&H signal except that it is now in quantised form.
- 14.Observe the output of the Low Pass Filter (3.4 KHz cut off frequency) which is replica of the input Analog Signal.

2. STUDY OF THE EFFECT OF AMPLITUDE VARIATION OF MODULATING SIGNAL

1. Observe the Analog input to PCM modulator and the output of PCM Demodulator on 2 channels of the Oscilloscope.
2. Increase the Amplitude by means of Potentiometer P_2 . The Amplitude is limited to $\pm 2.5V$ p-p only. The output will be reproduced undistorted.
3. Any further increase will saturate the ADC levels and the output peaks are flattened.
4. Decrease the Amplitude. The output signal amplitude will be reduced accordingly. Since lesser levels are there in the Sine wave at lower levels, some distortion is observed even after filtering.

3. STUDY OF SAMPLING FREQUENCY ON THE OUTPUT

The Analog Signal frequency (1KHz) and Sampling frequency (8KHz) are restored using Oscilloscope before starting this part of the experiment.

1. In each cycle of the Analog input we observe that there are about 8 Sampling Pulses. Thus the PCM Demodulated output is a true replica of input as observed on both the channels of the Oscilloscope.
2. Gradually reduce the Clock frequency using potentiometer P_4 which reduces the Sampling frequency. As the frequency decreases, the Sine wave output at one point gets so distorted that it does not resemble a Sine wave. Measure the Sampling frequency at this point. It is found that the frequency is 2KHz or even less as indicated by the Nyquist Theorem.

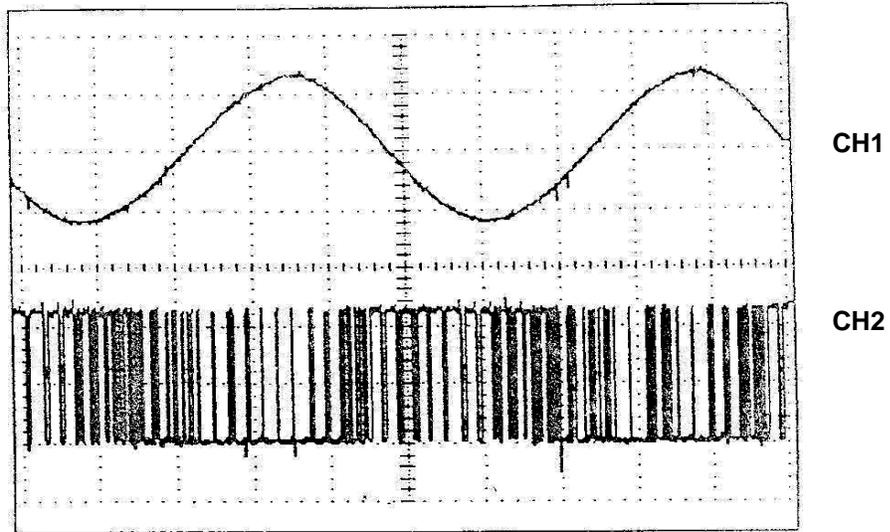
Usually for better reproduction, the Sampling frequency should be much more than the Nyquist Rate.

HARDWARE SPECIFICATIONS

1. Pulse Code Modulation and Demodulation Trainer Kit.
2. Built in DC power supply $\pm 12V$, $\pm 5V$ / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084, 7404, 74163, 555, 8038, 74164, 74165, 74374, DAC 0800, ADC 0800, CD 4053.
5. Set of Patch chords Stackable 2mm - 10 Nos.
6. User Manual.

CH1 : 2.000 V / div 1.000 us/div
CH2 : 2.000 V / div 1.000 us/div

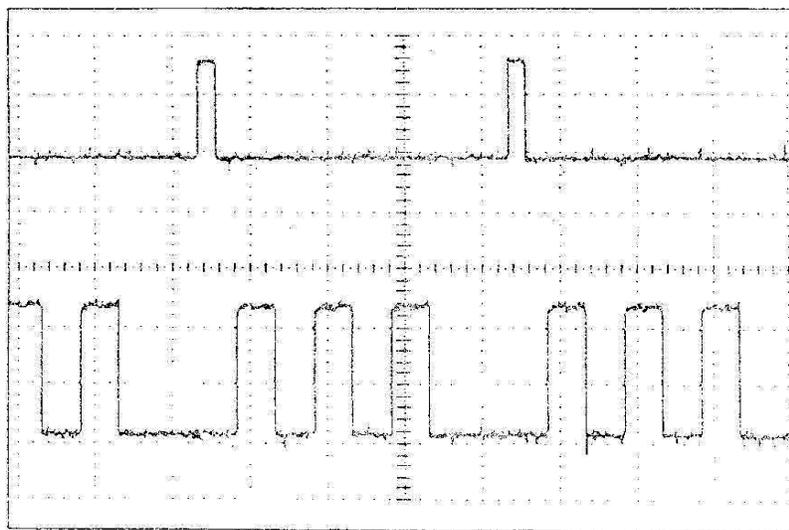
MODULATING SIGNAL INPUT



PULSE CODE MODULATED DATA OUT

CH1: 2.000 v/div 50.00 us/div
CH2: 2.000 v/div 50.00 us/div

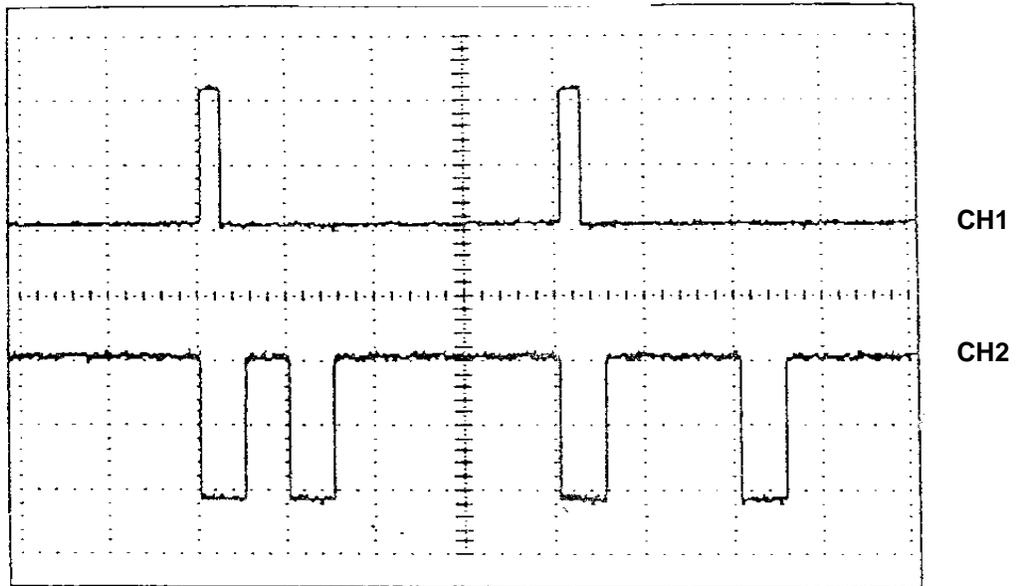
SAMPLING FREQUENCY



PCM COUTPUT FOR D.C. INPUT

CH1 : 2.000 V / div 50.00 us/div
CH2 : 2.000 V / div 50.00 us/div

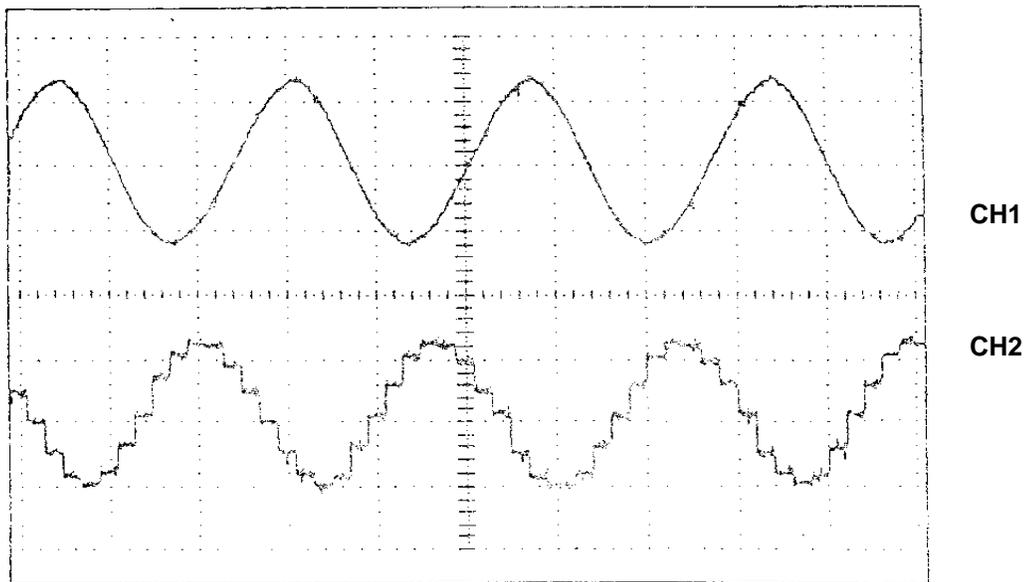
SAMPLING FREQUENCY



PCM OUTPUT FOR SINE WAVE I/P

CH1: 2.000 v/div 2.000ms/div
CH2: 5.000 v/div 2.000ms/div

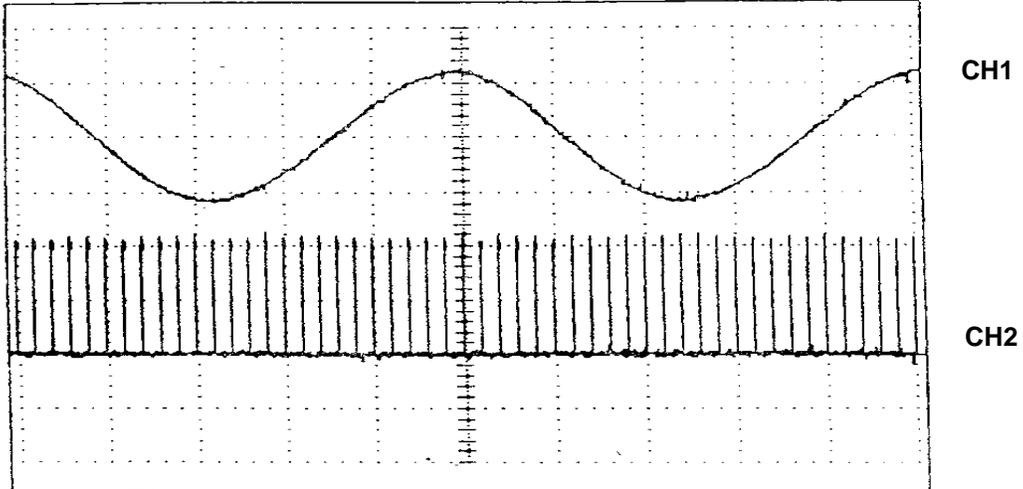
INPUT MODULATING SIGNAL



D+ TO -A CONVERTER OUTPUT

CH1 : 2.000 V / div 1.000 us/div
CH2 : 2.000 V / div 1.000 us/div

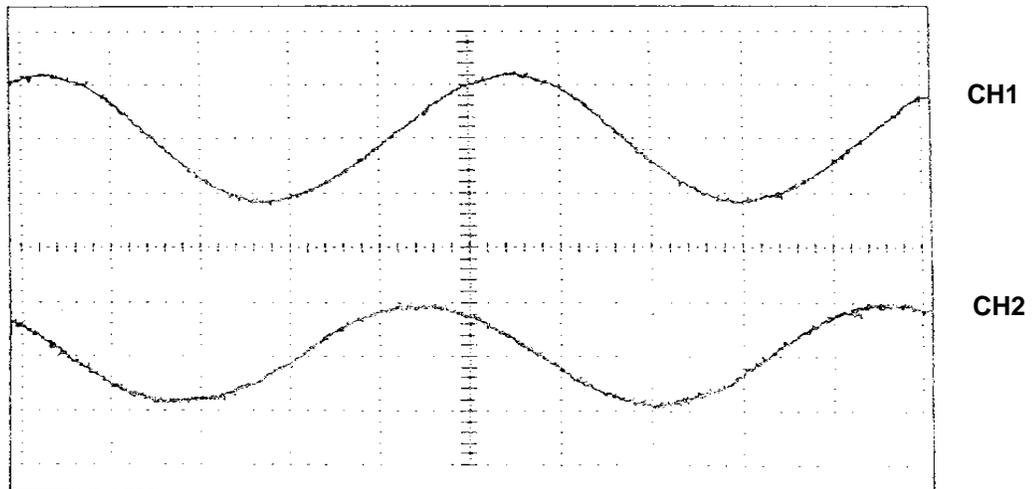
MODULATING SIGNAL INPUT



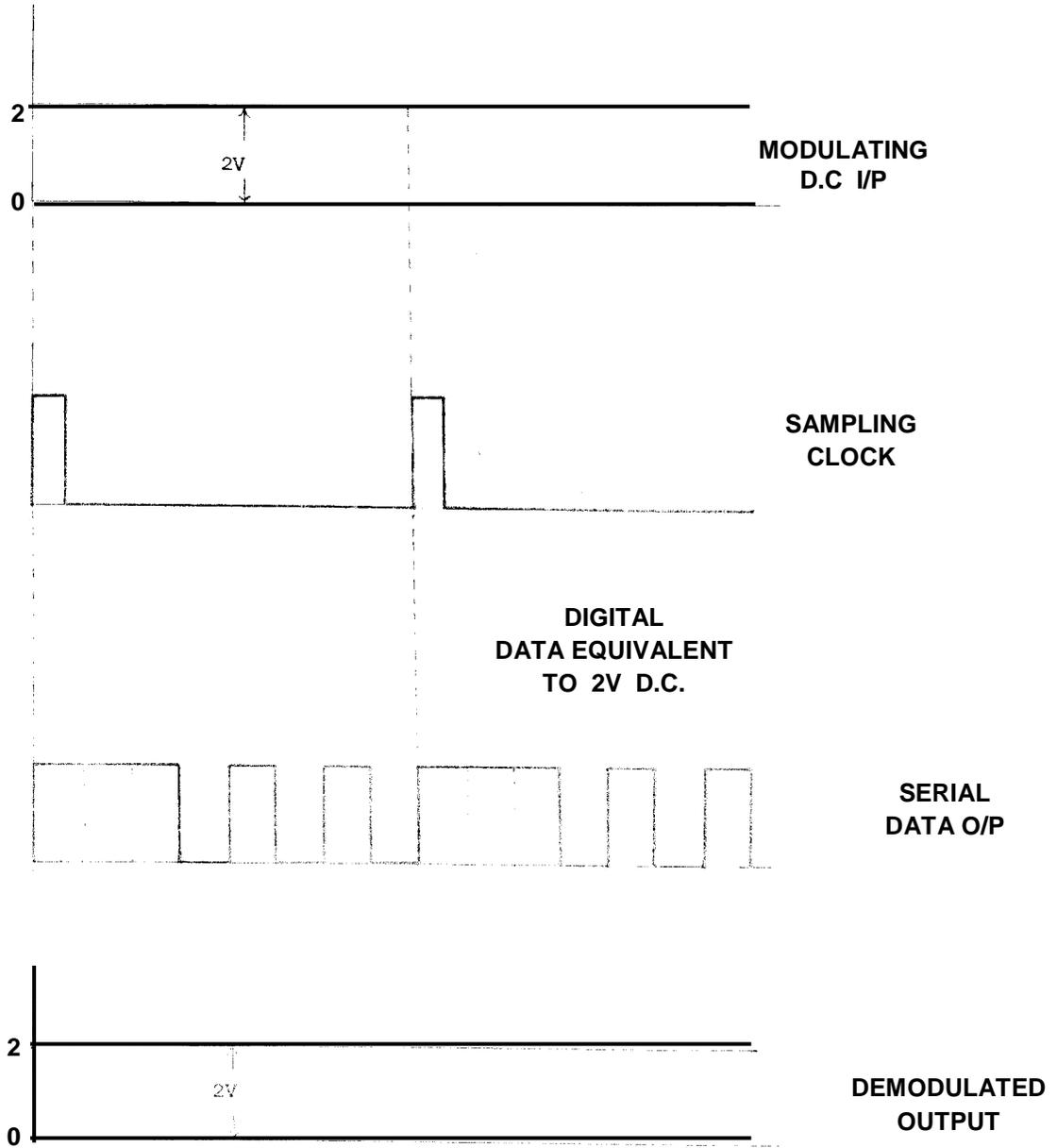
SAMPLING FREQUENCY

CH1: 2.000 v/div 1.000ms/div
CH2: 2.000 v/div 1.000ms/div

MODULATING SIGNAL INPUT



DEMODULATED OUTPUT



DIFFERENTIAL PULSE CODE MODULATION & DEMODULATION

AIM

To study Differential Pulse Code Modulation & Demodulation by sending variable frequency sine wave and variable D.C signal inputs.

INTRODUCTION

Pulse Code Modulation (PCM) is different from Amplitude Modulation (AM) and Frequency Modulation (FM) because, those two are continuous forms of modulation. Pulse Code Modulation (PCM) is used to convert analog signals into binary form. In the absence of noise and distortion it is possible to completely recover a continuous analog modulated signals. But in real time they suffer from transmission distortion and noise to an appreciable extent. In the PCM system, groups of pulses or codes are transmitted which represent binary numbers corresponding to Modulating Signal Voltage levels. Recovery of the transmitter information does not depend on the height, width, or energy content of the individual pulses, but only on their presence or absence. Since it is relatively easy to recover pulses under these conditions, even in the presence of large amounts of noise and distortion, PCM systems tend to be very immune to interference and noise. Regeneration of the pulse enroute is also relatively easy, resulting in system that produces excellent result for long-distance communication.

Differential PCM is quite similar to ordinary PCM. However, each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value as in normal PCM.

The rational behind this system is that speech is redundant, to the extent that each amplitude is related to the previous amplitude, so that large variations from one sample to the next are unlikely. This being the case, it would take fewer bits to indicate the size of the amplitude change than the absolute amplitude, and so a smaller bandwidth would be required for the transmission. The differential PCM system has not found wide acceptance because complications in the encoding and decoding process appear to out weigh any advantages gained.

DPCM ENCODING

DPCM Encoding is similar to the PCM encoding, except that initial stage employs Delta Modulation after that PCM encoding is following.

The encoding process generates a binary code number corresponding to Modulating signal voltage level to be transmitted for each sampling interval. Any one of the codes like binary, ASCII etc, may be used as long as it provides a sufficient number of different symbols to represent all of the levels to be transmitted. Ordinary binary number will contain a train of '1' and '0' pulses with a total of $\log_2 N$ pulses in each number. (N is no of levels in the full range). This system is very economical to realise, because it corresponds exactly to the process of analog - to- digital (A / D) conversion.

QUANTIZATION

The first step in the PCM system is to quantize the modulating signal. The modulating signal can assume an infinite number of different levels between the two limit values which define the range of the signal. In a PCM, a coded number is transmitted for each level sampled in the modulating signal. If the exact number corresponding to the exact voltage were to be transmitted for every sample, an infinitely large number of different code symbols would be needed. Quantization has the effect of reducing this infinite number of levels to a relatively small number which can be coded without difficulty.

In the quantization process, the total range of the modulating signal is divided up into a number of small subranges. The number will depend on the nature of the modulating signals and will form as few as eight to as many as 128 levels. A number that is an integer power of two is usually chosen because of the ease of generating binary codes. A new signal is generated by producing, each sample, a voltage level corresponding to the midpoint level of the subrange in which the sample falls. Thus if a range of 0 to 5V were divided into 128, 5/128V subranges, and the signal sampled when it was 3V, the quantizer would put a voltage of 2.96V and hold that level until the next sampling time. The result is a stepped wave form which follows the contour of the original modulating signal with each step synchronised to the sampling period Fig.1 illustrate the quantization process

QUANTIZATION NOISE

The quantized staircase waveform is an approximation to the original waveform. The difference between the two waveform amounts to "noise" added to the signal by the quantizing circuit. The mean square quantization noise voltage has a value of

$$E_{nq}^2 = \frac{S^2}{12} \quad \text{-----(1)}$$

where S is the voltage of each step, or the subrange voltage span. As a result, the number of quantization levels must be kept high in order to keep the quantization noise below some acceptable limit, given by the power signal-to-noise ratio, which is the ratio of average noise power. For a sinusoidal signal which occupies the full range, the mean square signal voltage is

$$E_s^2 = \frac{1}{2} \quad E_{Peak}^2 = \frac{1}{2} \quad \frac{(MS)^2}{2} = \frac{(MS)^2}{8} \quad \text{-----(2)}$$

where M is the number of steps and S is step height voltage. The signal-to-noise ratio is now given by

$$\frac{\text{Signal}}{\text{Noise}} = \frac{E_s^2}{E_{nq}^2} = \frac{(MS)^2}{8} \times \frac{12}{S^2} = \frac{3M^2}{8} \quad \text{-----(3)}$$

The number of levels M is related to the number n of bits per level by

$$M = 2^n$$

Substituting this in Eq.(3) gives, for the signal-to-noise ratio,

$$\frac{\text{Signal (S)}}{\text{Noise (N)}} = \frac{1}{2} \times 2^{2n}$$

In decibels this becomes

$$(S/N) \text{ dB} = 10 \log \left(\frac{3 \times 2}{2} \right)^{2n}$$

$$= 1.761 + 6.02n \text{ dB}$$

$$n = 7 \text{ bits}$$

$$\text{then } (S/N) \text{ dB} = 1.761 \times 6.02 \times 7 = 43.9 \text{ dB}$$

DECODING

The decoding process reshapes the incoming pulses and eliminates most of the transmission noise. A serial to parallel circuit passes the bits in parallel groups to a digital to analog converter (D/A) for decoding. Thus decoded signal passes through a sample and hold amplifier which maintains the pulse level for the duration of the sampling period, recreating the staircase waveform approximation of the modulating signal. A low-pass filter may be used to reduce the quantization noise.

BLOCK DIAGRAM DESCRIPTION

The block diagram of Differential Pulse Code Modulation and Demodulation is shown on front panel.

MODULATING SIGNAL

A variable sinusoidal frequency generator is provided with frequency from '100' Hz to 500 Hz. To see the actual bits that are transmitted through the communication channel.

DPCM ENCODING

The modulating signal is applied to the input of Analog-to-Digital (A/D) converter which performs the two functions of quantization and encoding, producing a 8-bit binary coded number. The signal is to be transmitted i.e., modulating signal is sampled at regular intervals.

If the maximum amplitude +5V is represented by 8-bits the 1LSB corresponds to $V \times \frac{1}{128} = 5/128 = 39 \text{ mV}$ and MSB represents the sign. So the values of the sampled signal at the output of Analog-to-Digital converter for Fig.2 are 0000000, 00111111, 01111111, 00111111, 00000000, 10111111, 11111111, 10111111, 00000000.

To transmit all the bits in channel one channel, actually it is often sent as binary number back to front by parallel to serial converter, i.e., 0000000 111111100 11111110 to make demodulating easier. A parallel to serial converter transmits the code bits in serial fashion.

DPCM DECODING

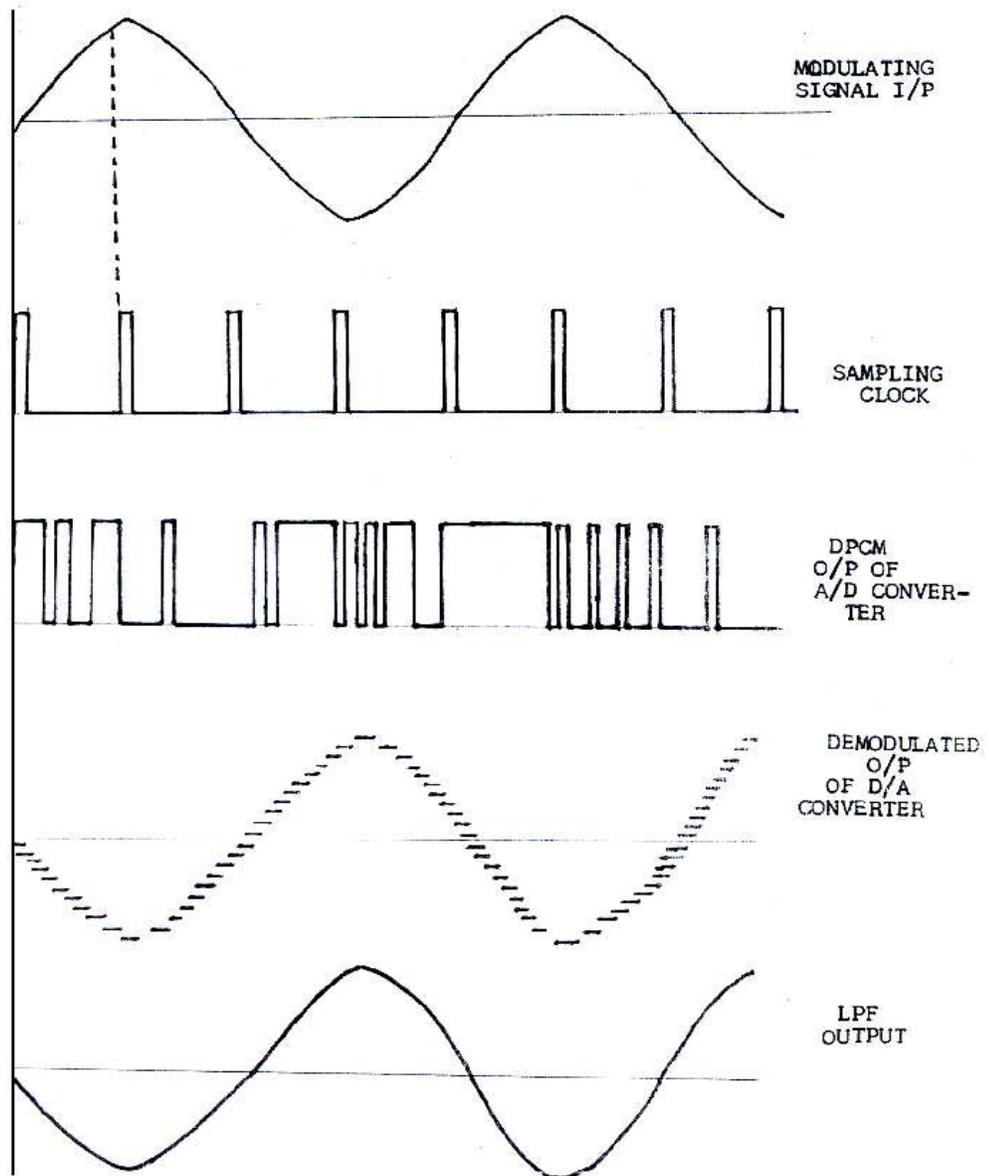
At the receiver end the received data will be in serial form. The serial data is converted back to parallel form by serial to parallel converter and passes the bits to a Digital-to-Analog converter for decoding which has in-built sample and hold amplifier which maintains the pulse level for the duration of the sampling period, recreating the pulse level for the duration of the sampling period, recreating the staircase wave form which is approximation of modulating signal. A low pass filter may be used to reduce the quantization noise and to yield the original modulating signal.

HARDWARE SPECIFICATIONS

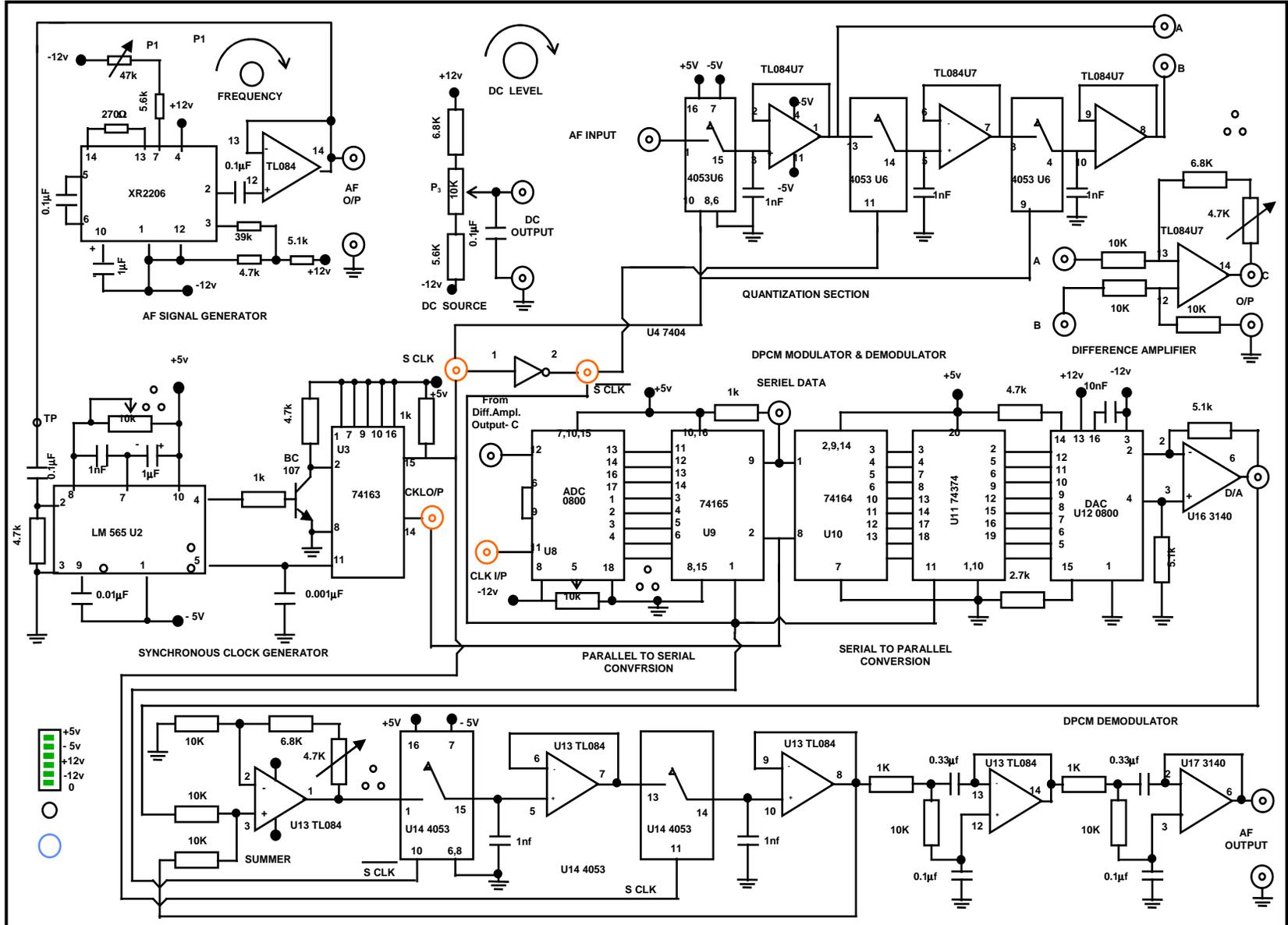
1. AF oscillator with variable Amplitude.
2. Variable D.C Source.
3. DPCM Modulator.
4. DPCM Demodulator.

EXPERIMENTAL PROCEDURE

1. Switch 'ON' the experimental kit.
2. Connect AF output to channel 1 of oscilloscope and also connect AF oscillator output to AF input of quantization section and connect S clock and S clock to the input terminals of quantization section.
3. Observe the outputs of two different sample and hold outputs at A and B.
4. Connect A and B outputs to difference amplifier and observe the differential output C on channel 2.
5. Apply differential output C, B clk, S clock and S clock to the input terminals of DPCM modulator section.
6. Observe the DPCM output serial data and D/A output on channel 2.
7. The D/A output is given to summer and the summer output is filtered by low pass filter to give AF output.
8. Now, disconnect the differential data and apply the variable DC signal to the input of the DPCM modulator
9. By adjusting the DC voltage potentiometer we can get the DPCM output from 0000 0000 to 1111 1111



FT 1510 DIFFERENTIAL PULSE CODE MODULATION & DEMODULATION



FUTURE TECH

Panel layout diagram

DELTA MODULATION & DEMODULATION

AIM

To study the Delta Modulation process by comparing the present signal with the previous signal of the given Modulating signal.

INTRODUCTION

In radio transmission, it is necessary to send audio signal (e.g. Music, speech etc.) from a broadcasting station over great distances to a receiver. This communication of audio signal which does not employ any wire and is sometimes called wireless. The audio signal cannot be sent directly over the air for appreciable distance. Even if the audio signal is converted into electrical signal, the latter cannot be sent very far without employing large amount of power. The energy of a wave is directly proportional to its frequency. At audio frequencies (20Hz to 20KHz), the signal power is quite small and radiation is not practicable.

The radiation of electrical energy is practicable only at high frequencies e.g. Above 20KHz. The high frequency signals can be sent thousands of miles even with comparatively small power. Therefore, if audio signal is to be transmitted properly, some means must be devised which will permit transmission to occur at high frequencies while it simultaneously allows the carrying of audio signal. This is achieved by imposing electrical audio signal on high frequency carrier/ The resultant waves are known as modulated waves or radio waves and the process is called modulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process called demodulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process called demodulation. The signal is then amplified and reproduced into sound by the loudspeaker.

MODULATION

A high frequency carrier wave is used to carry the audio signal which is done by changing some characteristic of carrier wave in accordance with the signal. Under such conditions, the audio signal will be contained in the resultant wave. The process is called modulation and defined as "The process of changing some characteristic (e.g. Amplitude, Frequency or Phase) of a carrier wave in accordance with the intensity of the signal is known as Modulation".

Modulation means to "change". In modulation, some characteristic of a carrier wave is changed in accordance with the intensity (i.e. Amplitude) of the signal. The resultant wave is called modulated wave or radio wave and contains the audio signal. Therefore, modulation permits the transmission to occur at high frequency while it simultaneously allows the carrying of the audio signal.

NEED FOR MODULATION

Modulation is extremely necessary in communication system due to the following reasons.

1. PRACTICAL ANTENNA LENGTH : In order to transmit a wave effectively, the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$\text{Now Wavelength} = \frac{\text{Velocity}}{\text{frequency}} = \frac{3 \times 10^8}{\text{frequency (Hz)}} \text{ meters}$$

As the audio frequencies range from 20Hz to 20KHz, therefore, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For instance, to radiate a frequency of 20KHz directly into space, we would need an antenna length of $3 \times 10^8 \div 20 \times 10^3 = 15,000$ meters. This is too long antenna to be constructed practically. For this reason, it is impracticable to radiate audio signal directly into space. On the other hand, if a carrier wave say of 1000KHz is used to carry the signal, we need an antenna length of 300 meters only and this size can be easily constructed.

2. OPERATING RANGE

The energy of a wave depends upon its frequency. The greater the frequency of the wave, the greater the energy possessed by it. As the audio signal frequencies are small, therefore these cannot be transmitted over large distances if radiated directly into space. The only practical solution is to modulate a high frequency carrier wave with audio signal and permit the transmission to occur at this high frequency (i.e carrier frequency).

3. WIRELESS COMMUNICATION

One desirable feature of radio transmission is that it should be carried without wires i.e. Radiated into space. At audio frequencies radiation is not practicable because the efficiency of radiation is poor. However, efficient radiation of electrical energy is possible at high frequencies. For this reason, modulation is always employed in communication systems.

INTRODUCTION

Delta Modulation is a Differential Pulse Code Modulation Technique, in which the difference signal between two successive samples is encoded into a single bit code.

Fig-1 shows the block diagram of the Delta Modulation. This is also known as Linear Delta Modulator. The signal $m(t)$ is the analog input signal. While $r(t)$ is a reconstructed signal which is same as the quantised input signal with 1 bit delay. The signal $r(t)$ tries to follow the input signal $m(t)$ with one bit period delay.

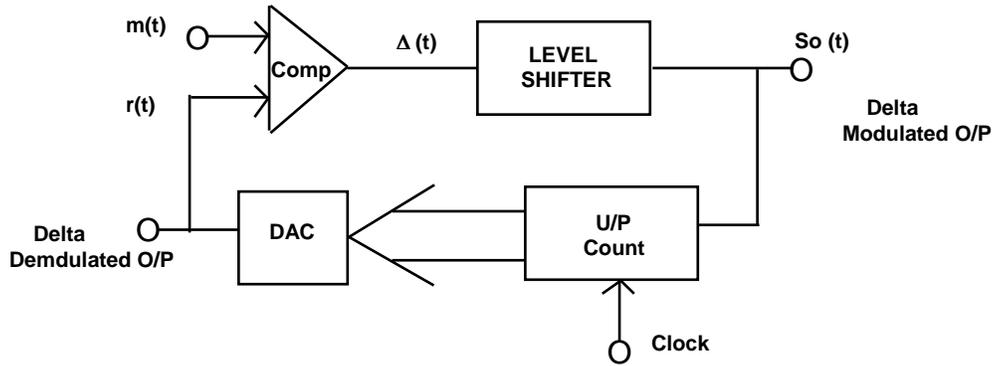


FIG - 1 BLOCK DIAGRAM OF DELTA MODULATION

THEORY

The process of encoding is as follows. The comparator compares the input signal $m(t)$ and $r(t)$. If $m(t) > r(t)$ a logic 1 is generated at the output of the comparator, otherwise a logic 0 is generated. The value of logic 1 or logic 0 turned as $\Delta(t)$ is held for the bit duration by the sample and hold current to generate $S_o(t)$, the Delta Modulated Output.

This output $S_o(t)$ is fed to the 8 bit binary up/down counter to control its count direction. A logic 1 at the mode control input increases the count value by one and a logic '0' decrements the count value by one. All the 8 outputs of the counter are given to DAC to reconstruct the original signal. In essence the counter & Decoder forms the Delta Modulator in the feedback loop of the comparator. Thus, if the input signal is higher than the reconstructed signal the counter increments at each step so as to enable the DAC output to reach to the input signal values. Similarly if the input signal $m(t)$ is lower than the reconstructed signal $r(t)$, the counter decrements at each step, and the DAC output gets reduced to reach a value to that of $m(t)$.

The block diagram of Delta demodulator is shown below. It works in the same way as it was in the feedback loop of the Delta modulator. The received Delta modulated signal $S_o(t)$ is given to the mode control input (U/ D) of the up/ down counter. The counter is 8 bit wide and counts in binary fashion. All the 8 outputs are connected to an 8 bit DAC which gives a quantised analog signal (stepped waveform). A low pass filter is used to smooth out the steps. A buffer amplifier provides the necessary drive capability to the output signal. Thus the digital Delta modulated data is demodulated and reconstructed into an analog signal.

Although this process of Delta Modulation and Demodulation is a simple and cost effective method of coding, there will be poor approximation at starting buildup and 'hunting' at flat top signals.

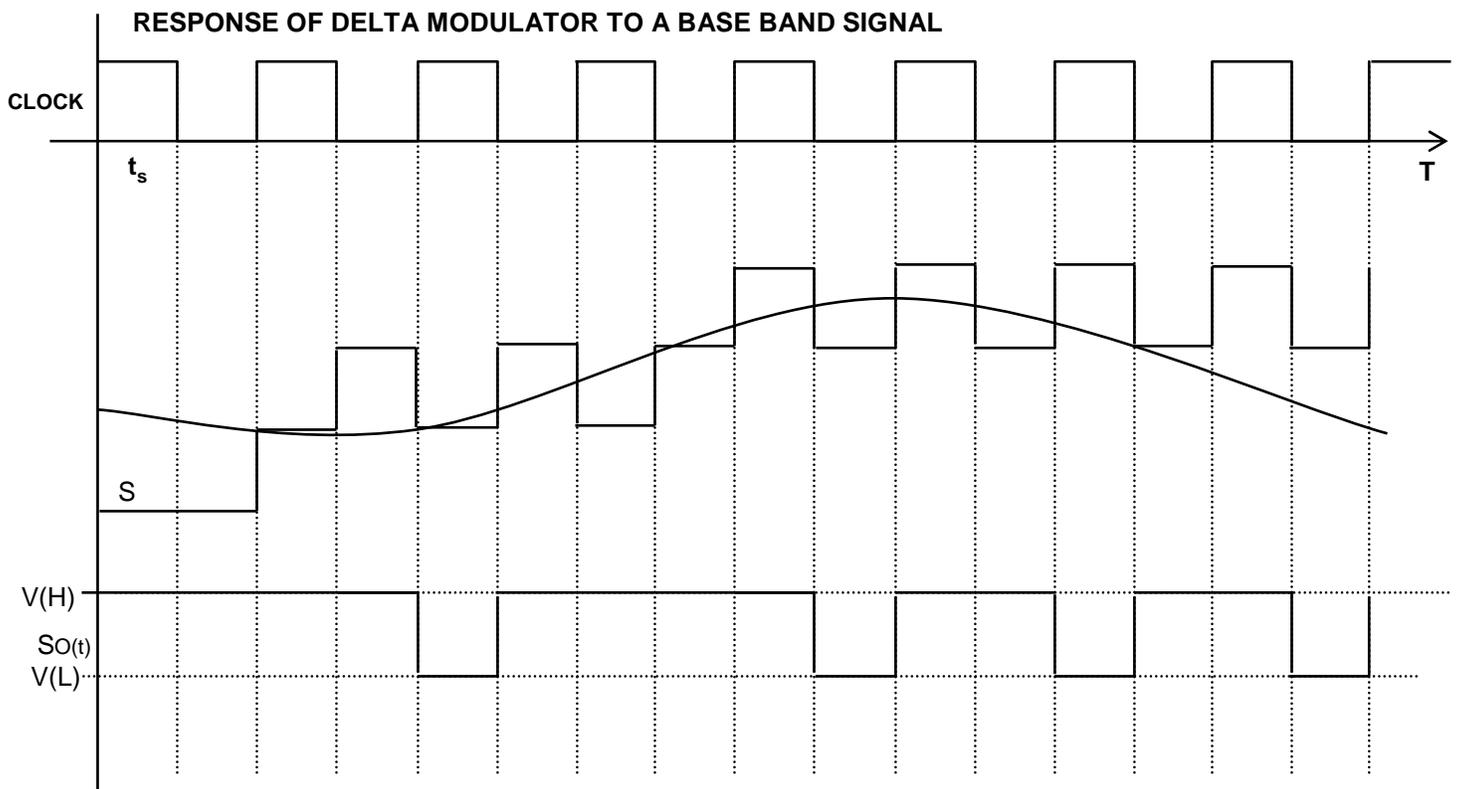


Fig - 2

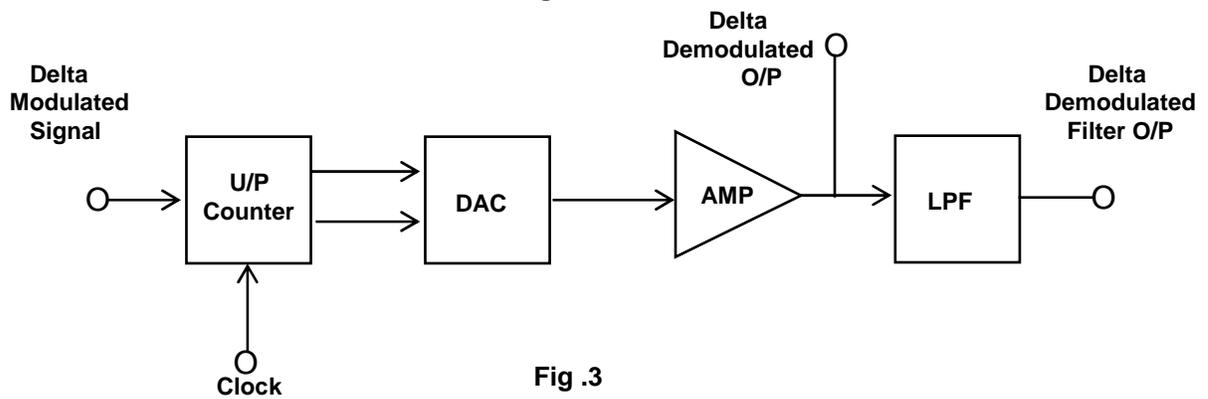


Fig .3

RESPONSE LIMITATIONS OF DELTA MODULATION

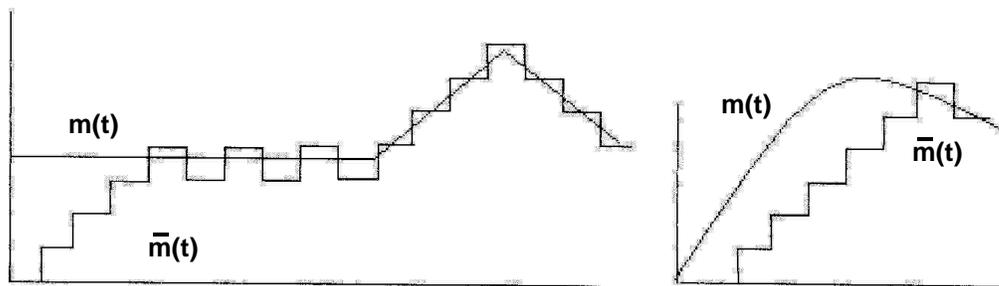


Fig .4

Another limitation in Delta Modulation is ' slope overloading;. Basically the DAC can produce a Max. signal variation of (256×5) volts in 256 clock pulses where is the quantisation step size T_c is the clock period the max. Slope that the DAC can produce in S/T_s volts / second which is the limiting factor where S is the step size and t_s is clock period. If the input signal slope is higher than this or in other words, if the input signal frequency is greater than the limiting value, slope overloading occurs. In such a case true reproduction of the analog signal is not possible. A sinusoidal waveform of amplitude A & frequency f has a maximum slope of $2\Delta fA$ which occurs at zero crossing of the sine wave. If the overloading is to be avoided then the following condition should be satisfied.

$$S_f > / 2\pi fA$$

When S = quantisation step size,

f_s = sampling frequency (Bit frequency), f = Signal frequency , A = Signal Amplitude

$$f_s = \frac{2 \pi fA}{S} = \frac{\pi f 2A}{S}$$

When $2A$ = Peak to Peak Amplitude

= $256 \times s$ = DAC Max. Amplitude

$$f_s = \pi f \times 256 = 256 \pi f$$

For a signal frequency of 200Hz, the sampling frequency should be

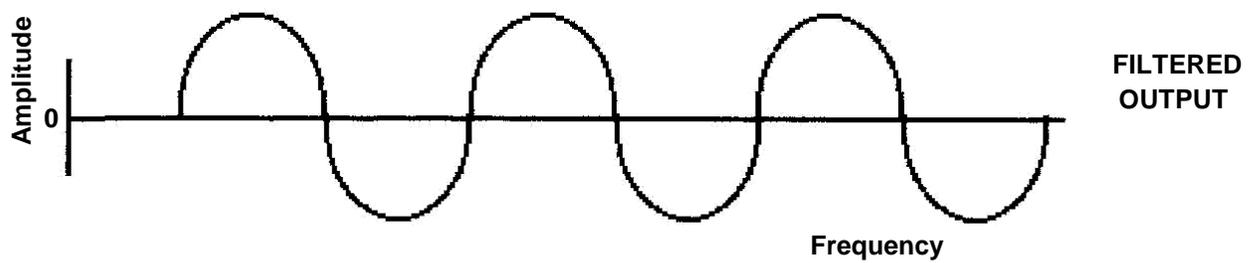
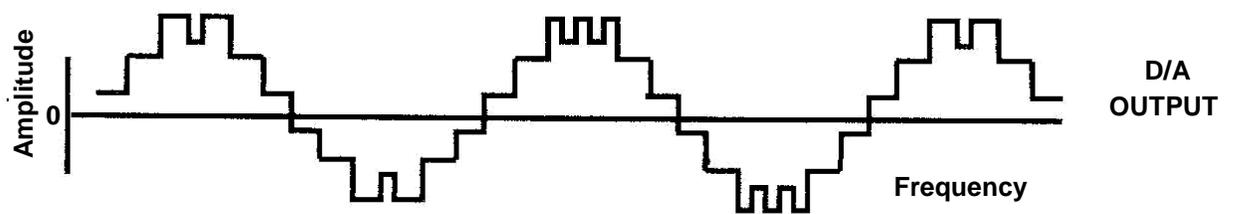
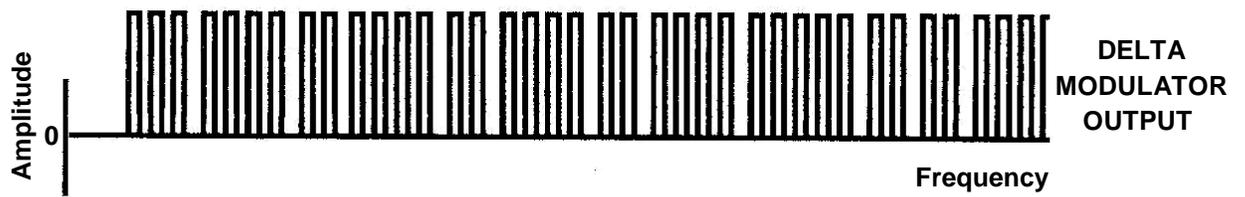
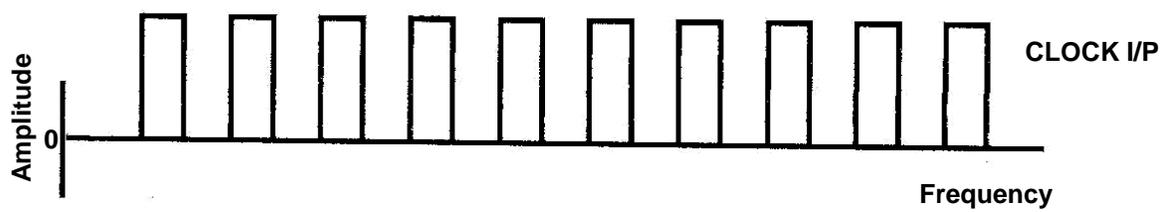
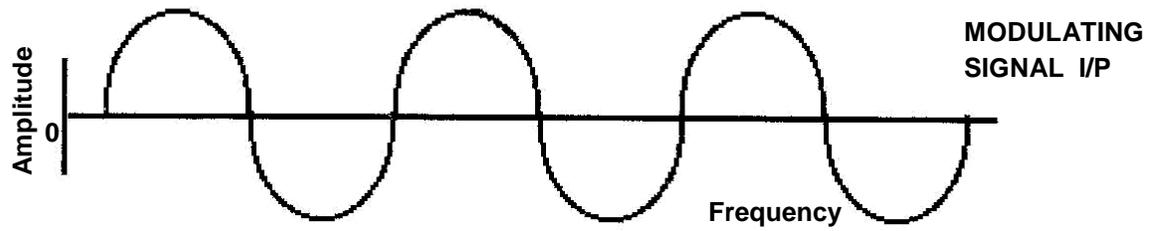
$$f_s = 256 \times \pi \times 200 = 160\text{KHz}$$

HARDWARE SPECIFICATIONS

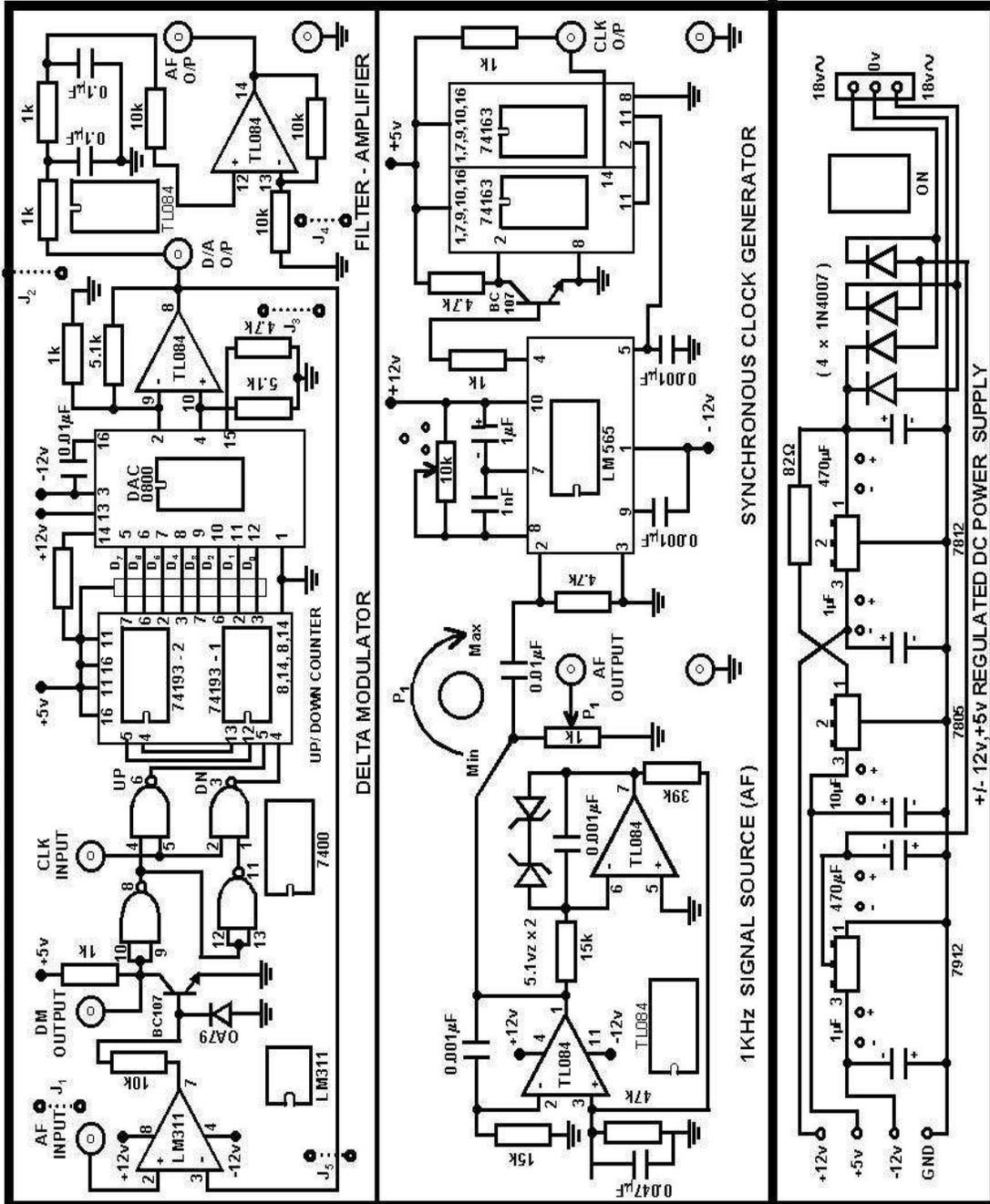
1. Delta Modulation and Demodulation Trainer.
2. Built in DC power supply + 5V / 350mA , +/- 12V / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084(1No), 555 (1No), (74193 (2 Nos), DAC0800(1 No) , 7400 (1 No) , LM 311 (1 No).
5. Set of Patch chords Stackable 2mm - 6 Nos.
6. User Manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Switch ON the experimental board.
3. Connect Clock Signal to the Delta Modulator circuit.
4. Connect Modulating Signal to the Modulating signal input of the Delta Modulator and observe the same on channel 1 of a Dual Trace Oscilloscope.
5. Observe the Delta Modulator output on channel II.
6. Connect this Delta Modulator output to the Demodulator.
7. Also connect the clock signal to the demodulator.
8. Observe the Demodulator output with and without RC filter on CRO.



FT 1511 DELTA MODULATION AND DEMODULATION



FUTURE TECH

PANEL DIAGRAM

PHASE SHIFT KEYING MODULATION & DEMODULATION

AIM

To study the operation of PHASE SHIFT KEYING modulation and demodulation .

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites. Phase Shift Keying (PSK) is a relatively new system, in which the carrier may be phase shifted by +180 degrees for a mark, and by -180 degrees for a space. PSK has a number of similarities to FSK in many aspects, as in FSK , frequency of the carrier is shifted according to the modulating square wave.

THEORY

Fig-1 shows the circuit diagram of the Phase Shift Key modulation and demodulation. In this carrier Generator is generated by a wein bridge oscillator around 28 KHz. At $\pm 5V_{p-p}$ sine wave using 741 IC. The sine wave is converted into square wave using TL084 in comparator mode. The transistor BC107 converts the square wave signal to TTL level. This is used as a basic bit clock or 180° for a mark and 0° for space. This square wave is used as a clock input to a decade counter (IC7490) which generates the modulating data outputs. IC CD4051 is an Analog multiplexer to which carrier is applied with and without 180° phase shift to the two multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered the output. The 180° phase shift to the carrier signal created by an operational amplifier using 741 IC. During the demodulation, the PSK signal is converted into a +5 volts square wave signal using a transistor and is applied to one input of an EX - OR gate. To the second input of the Logic gate, carrier signal is applied after conversion into a +5 volts signal. So the EX - OR gate output is equivalent to the modulating data signal.

Phase shift keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal (the carrier wave).

Any digital modulation scheme uses a finite number of distinct signals to represent digital data.

PSK uses a finite number of phases, each assigned a unique pattern of binary bits.

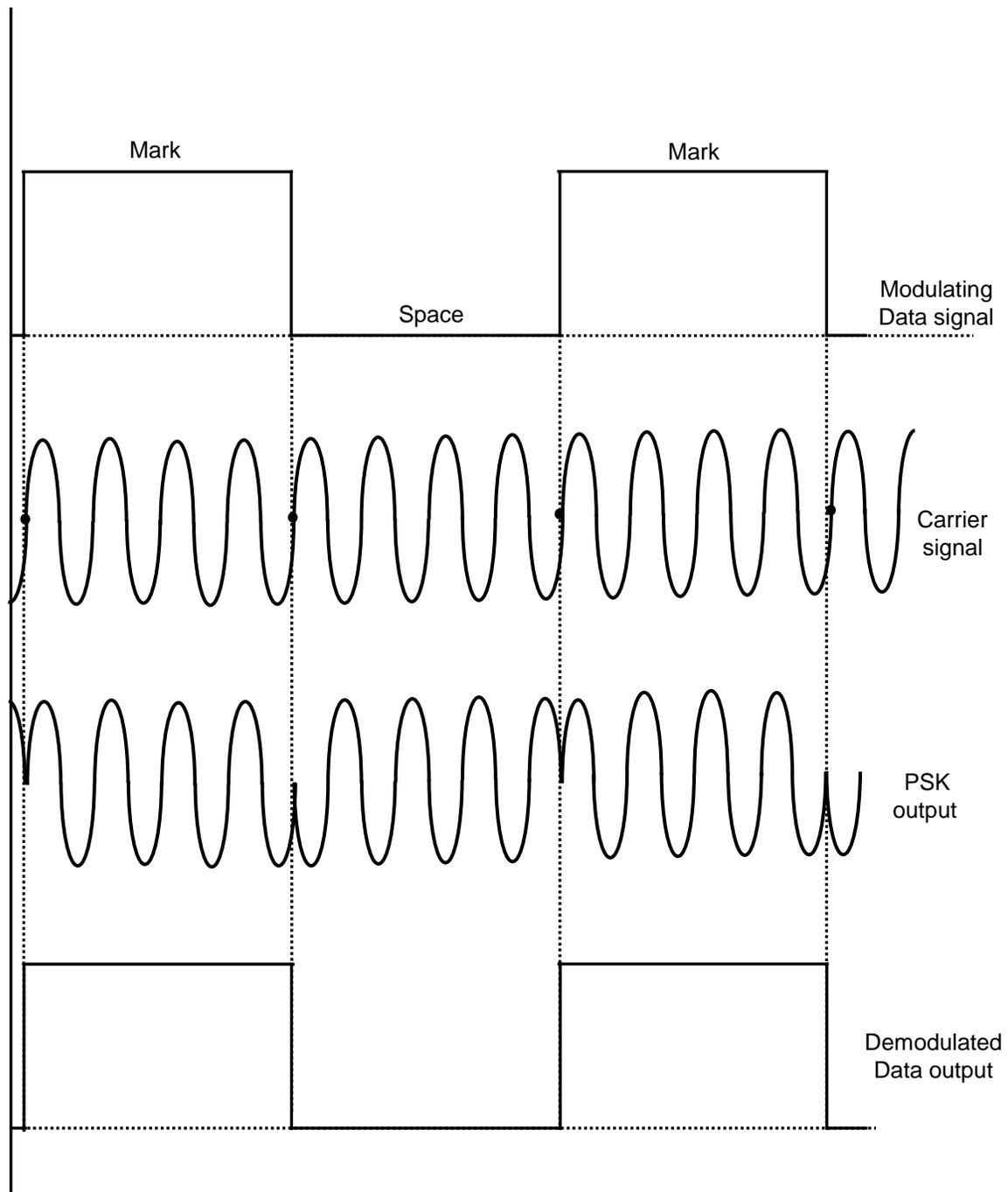
Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator, which is designed specifically for the symbol set used by the modulator determines the phase of the received signal and maps it back to the symbol it represents, thus recovering the original data. This requires the receiver to be able to compare the phase of the received signal to a reference signal.

HARDWARE SPECIFICATIONS

- 1) Panel layout diagram with components mounted on PCB / panel.
- 2) Built in DC power supplies $\pm 5V/ 350mA$.
- 3) Provided with 2mm sockets.
- 4) ICs provided on the board are 741, 7490, TL084, CD4051 & 7486.
- 5) Set of patch cords
 2mm Stackable patch cords – 8 Nos.
- 6) user manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Apply the carrier signal to the input of the modulator.
3. Apply the modulating data signal to the modulator input and observe this signal on channel 1 of the CRO.
4. Observe the output of the PSK modulator on the channel 2 of the CRO.
5. Apply this PSK output to the demodulator input and also apply the carrier input.
6. Observe the demodulator output and compare it with the modulating data signal applied to the modulator input which is identical.

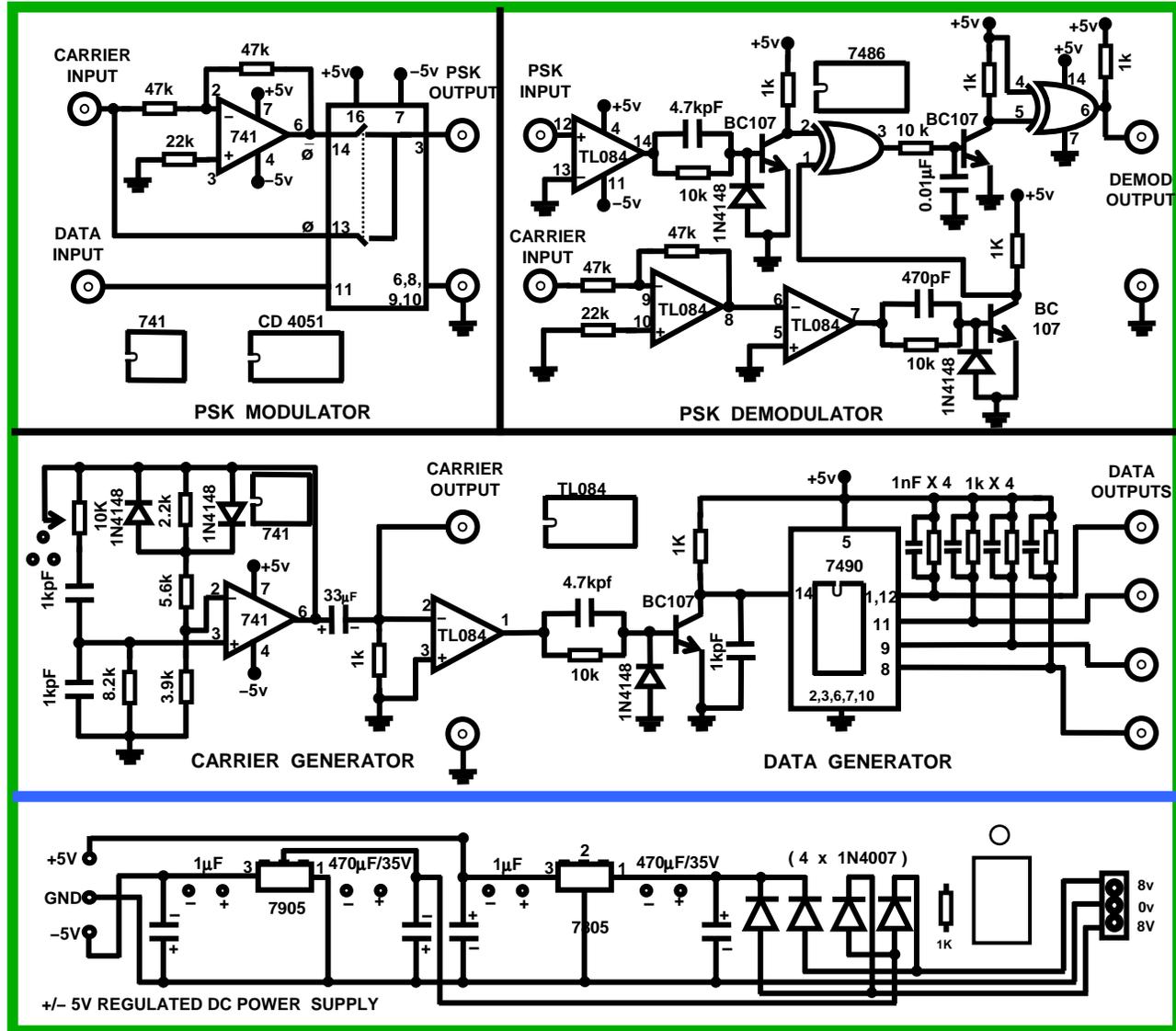


PSK Signal Waveforms

FUTURETECH

FT1507

PHASE SHIFT KEYING MODULATION & DEMODULATION



PANEL LAYOUT DIAGRAM

DIFFERENTIAL PHASE SHIFT KEYING MODULATION & DEMODULATION

AIM

To study the various steps involved in generating the differential binary signal and differential phase shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites.

Phase shift keying (PSK) is a relatively a new system, in which the carrier is phase shifted by + 90 degrees for a mark, and by -90 degrees for a space.

PSK has a number of similarities to FSK in many aspects, as in FSK, frequency of the carrier is shifted according to the modulating data level.

THEORY

The carrier wave signal is generated by a wein bridge oscillator around *** KHz at $\pm 5V$ P-P sine wave using 741 the sine wave is convert into square wave using TL084 in comparator mode. The Transistor BC 107 converts the square signal to TTL levels. This is used as a basic bit clock or 180° for a mark and 0° for space. This Square wave is used as a clock input to a decade counter (IC 7490) which generates the modulating data outputs.

MODULATION

The Differential signal to the modulating signal is generated using an Exclusive -OR gate (7486) and a 1-bit delay circuit using D Flip Flop 7474 (It is shown in fig-1). CD 4051 is an analog multiplexer to which carrier is applied with and without 180° degrees Phase shift (created by using an operational amplifier connected in inverting amplifier mode) to the input of the TL084. Differential signal generated by Ex-OR gate (IC7486) is given to the multiplexer's control signal input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. 1-bit delay generation of differential signal to the input is created by using a D-flip-flop(IC7474).

DEMODULATION

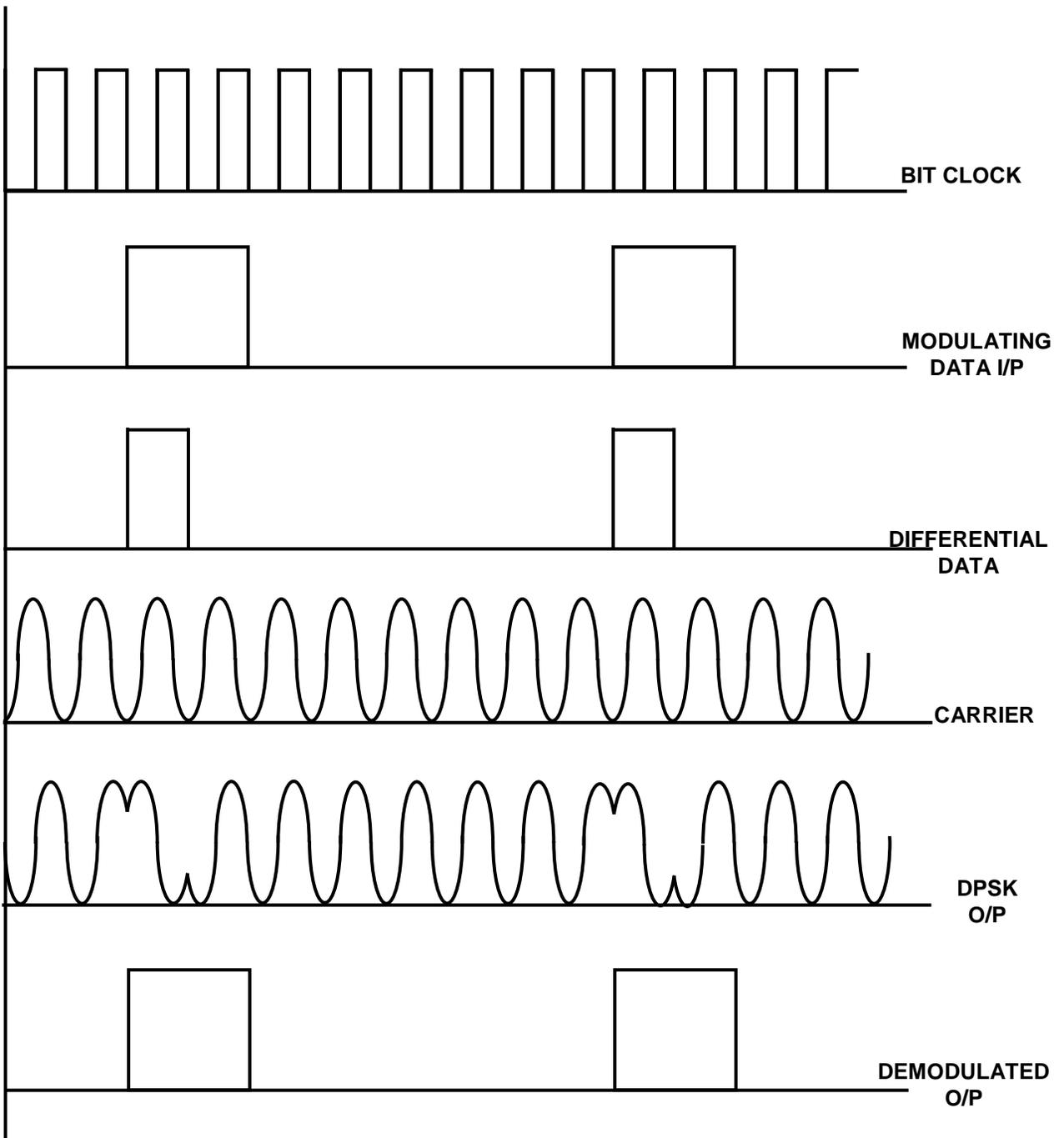
During the demodulation, the data and carrier are recovered through a TL084 op amp in comparator mode. This level is brought to TTL level using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5V signal. So the EX-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to one input of an Exclusive -OR gate and to the second input, after 1-bit delay the same signal is given. So the output of this Ex-OR gate is the recovered Modulating signal.

HARD WARE SPECIFICATIONS

1. Panel lay out diagram with components mounted on PCB /Panel
2. Built in variable DC power supplies $\pm 5V$, $\pm 350mA$, the figures given.
3. ICs 741, 7490, 7474, CD4051, 7486 are provided on the trainer and the hardware details are given.
4. User Manual
5. Set of patch chords

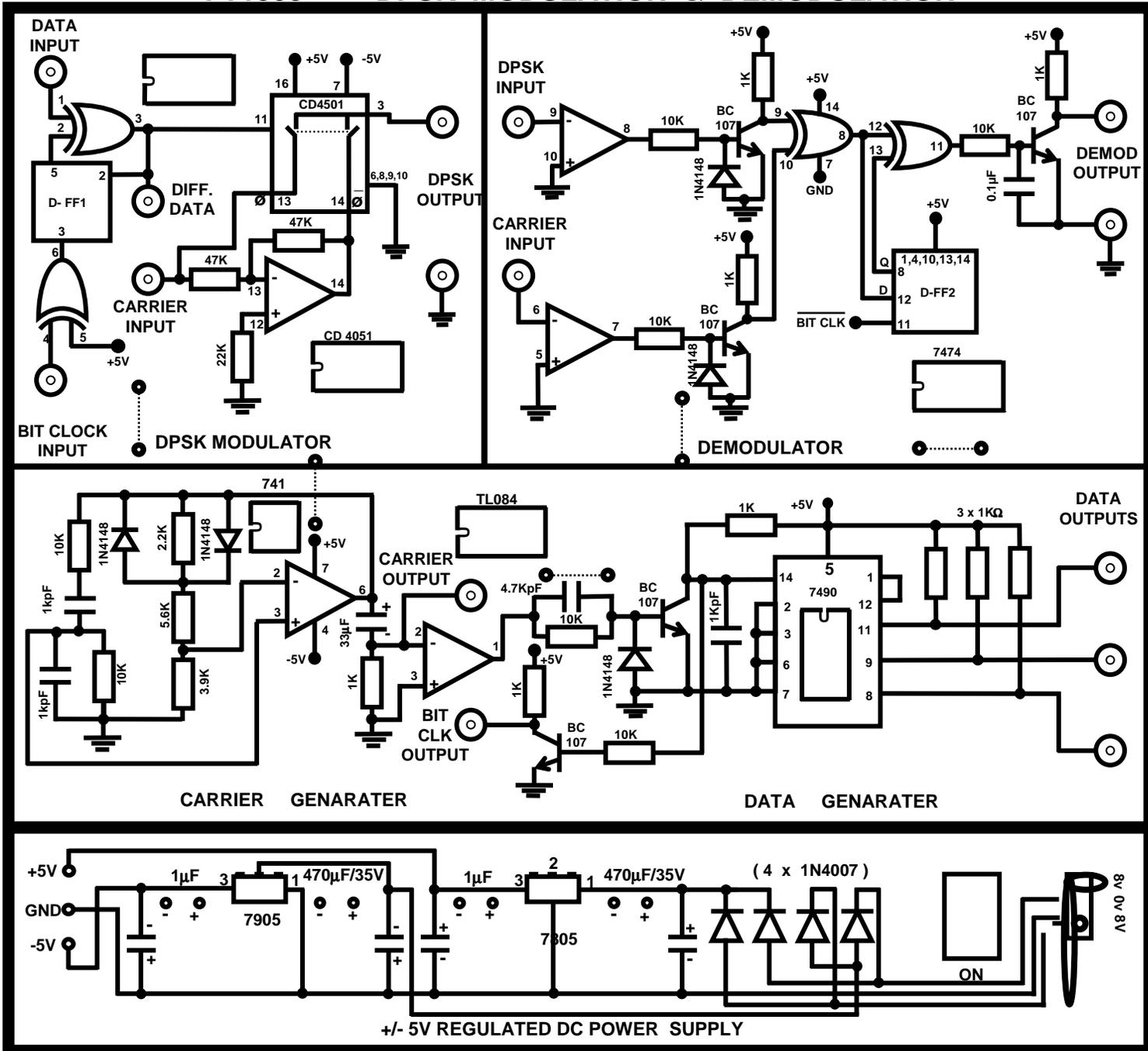
6.EXPERIMENTAL PROCEDURE

1. 'Switch ON' the experimental board.
2. Check the carrier signal and the data generator signals initially.
3. Apply the carrier signal to the carrier input of the DPSK modulator and give the data generator to the data input of DPSK modulator and bit clock output to the input of DPSK modulator and Bit Clk O/P to Bit Clk input of modulator.
4. Observe the DPSK modulating output with respect to the input data generator signal of dual trace oscilloscope (observe the DPSK modulating signal on channel 1 and the data generator signal on channel 2), and observe the DPSK Signal with respect to Differential data also.
5. Give the output of the DPSK modulator signal to the input of demodulator, give the bit clock output to the bit clock input to the demodulator and also give the carrier output to the carrier input of demodulator.
6. Observe the demodulator output with respect to data generator signal (modulating signal)



DPSK Signal Waveforms

FT1508 DPSK MODULATION & DEMODULATION



FREQUENCY SHIFT KEYING MODULATION & DEMODULATION

AIM

- 1 To study **FSK** Modulation Technique.
- 2 To study **FSK** Demodulation Technique.

HARWARE DESCRIPTION

- 1 HF clock sources $f_n = 100 \text{ Hz}$ to 100 kHz
- 2 Data Clock Generator
- 3 8 Bit Word Generator
- 4 SPDT Switches to select '0's & '1's
- 5 Carrier Signal Generator
 1. 5 kHz to 13.8 kHz When Data input is held low
 2. 13.15 kHz to 36.36 kHz When Data input is held high.
- 6 FSK Modulator.
- 7 FSK Demodulator
- 8 Built in Power supplies $\pm 12\text{V}$, $+5\text{V}$ @ 350 mA .

CIRCUIT DESCRIPTION

The Complete circuit diagram and the component layout is shown in Panel diagram.

1. HF CLOCK SOURCE

The Bit Clock source is designed around the popular timer IC 555 operated in Astable mode . The $1\text{M}\Omega$ Potentiometer in conjunction with $0.0047 \mu\text{F}$ condenser used as the timing circuit facilitates the frequency to be set & at any chosen value from 100 Hz to 100 kHz

2. DATA CLOCK GENERATOR.

A 74163 IC which is a Divide by -16 counter is provided to generate different data frequencies of $f/2, f/4, f/8$ & $f/16$ of the input clock frequency to this counter. The output frequencies are used as clock inputs to the 8 Bit word generator.

8 BIT WORD GENERATOR

The 8 Bit Parallel Load Serial Shift IC 74165 is used to generate the required word Pattern. A set of 8 DIP switches are used to set ONE & ZERO Pattern. The Bit Pattern set by the switches are parallely loaded by controlling the logic level at Pin 1. The last stage output Q_7 is coupled to the first stage input D_0 in the Shift Register. The Serial Shift Clock is given at Pin 2 from any one of the outputs of Data clock generator. The 8 Bit data set by the switches and loaded into the Register parallely is now shifted serially and circulated repetitively. Thus the 8 Bit word Pattern is generated cyclically which is used as modulating signal in the FSK Modulator.

SPDT SWITCHES TO SELECT '0's AND '1's

SPDT switches are provided to select the 8 Bit data from 0000 0000 to 1111 1111 a 8-Bit word generator. Output of the 8 Bit word generator is given as 'Data input' to the Modulator.

CARRIER SIGNAL GENERATOR / FSK MODULATOR

A 8038 IC based sine wave generator is provided as a carrier generator of frequencies of 5 KHz to 13.38 KHz, 13.15KHz to 36.36 KHz, when Data input is held low or High respectively . The output of the 8038 IC is given to a buffer amplifier, Which gives $0-8V_{p-p}$ sine wave output . The data input is given to a transistorised switch which drives f_m sweep input Pin No. 8 of 8038 IC. The TTL signal at the input of Transistor translates the level from 10V to 5V level to switch the sine wave frequency (carrier). These signals are the FSK modulated signals.

FSK DEMODULATOR

A diode detector with an input integrator and a low pass filter with a cut off frequency of 3.4 kHz is used to demodulate the FSK signal . The output of the low pass filter is given to an op Amp comparator. The output is the replica of the original data transmitted at the FSK modulator.

POWER SUPPLIES

Built - in + 5V , $\pm 12V$ @ 350 mA fixed D.C power supplies are provided in the system. A 230 V to 18-0-18V @ 750 mA step down transformer is provided and this AC signal is given to a full wave rectifier. The rectifier output is given to a capacitor input filter and + 12V @ 350mA regulator. In a similar way -12V @ 350 mA power supply . It also generated a second full wave rectifier from 8-0-8V AC and a regulator 7805 generates +5V DC @ 350mA .

EQUIPEMENT REQUIRED

- 1 Frequency Shift Key Modulation and Demodulation kit.
- 2 Oscilloscope - 20 MHz - Dual Channel.

EXPERIMENTAL PROCEDURE

- 1 Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
- 2 Connect 'Data Input's socket to ground
- 3 Connect the FSK output to the Ch1 of the Oscilloscope and trigger the scope from Ch1.
- 4 Set the 'Freq. Adj' Potentiometer So that the output is around 30 kHz approx.
- 5 Set the Switches for required word pattern.
Push the load switch momentarily and release . This will parallel load the word pattern and then shifts the pattern that is set Adjust the required frequency of the clock.
- 6 Connect the Data input to 'Ground', Measure the frequency.
- 7 Connect the 'Data output' to 'Data input' .
- 8 Observe the Data output on CH1 and FSK output on CH2.
- 9 Observe that at each negative transition' ' the carrier switches from high to low and every positive transition ' ' the frequency switches from low to high.

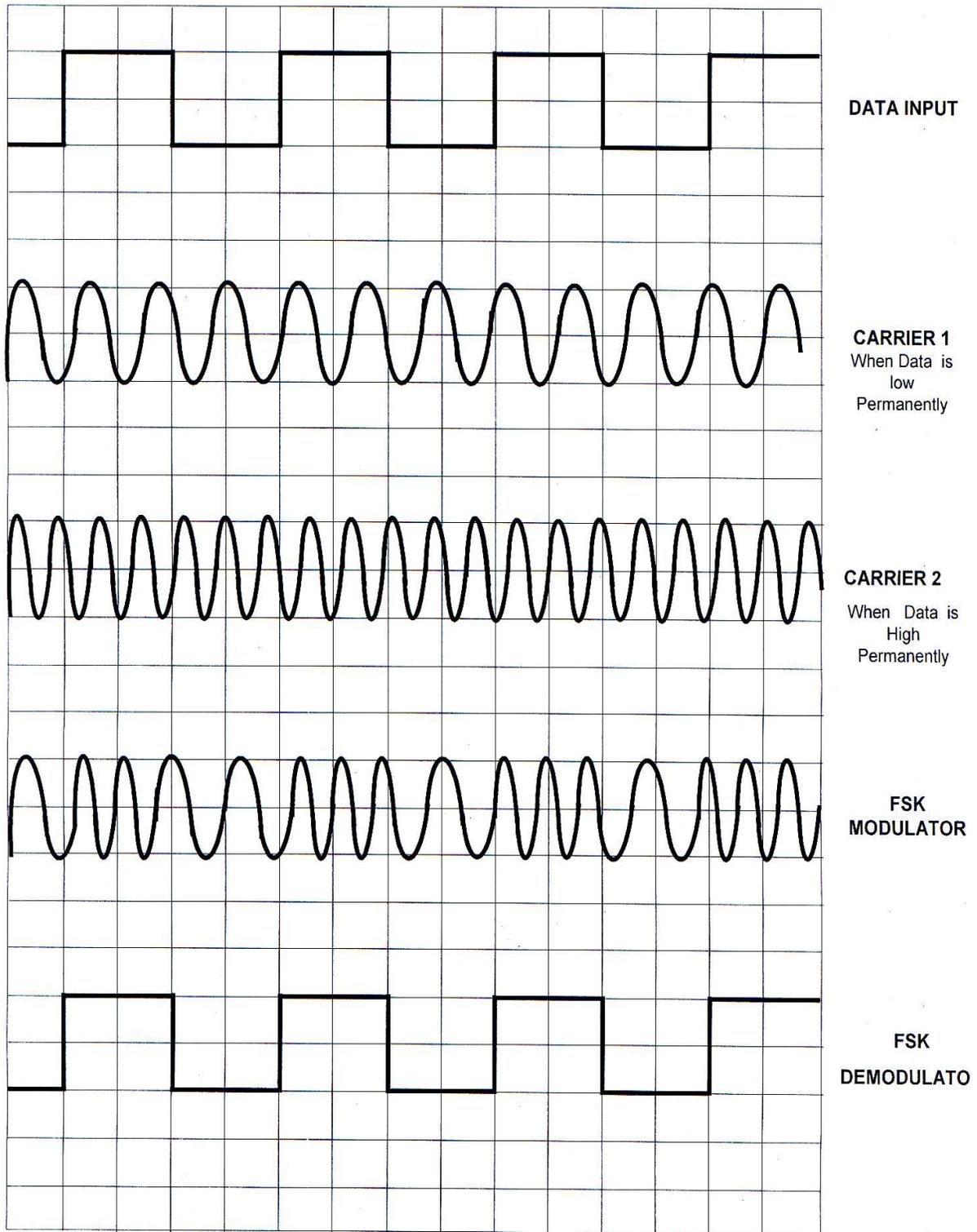
- 10 Connect 'FSK output ' to ' FSK input ' of the Demodulator.
- 11 Adjust P_3 to regenerate the Data correctly.
- 12 Compare the Demod output to the Data output which are identical in nature.
- 13 Change the Data Pattern as mentioned in sl No 6, and Observe the Demod output again.

HARD WARE SPECIFICATIONS

- 1 Frequency Shift keying Modulation & Demodulation Trainer kt.
- 2 Built - in Power supplies $\pm 12V$, $+5V$ / 350mA.
- 3 Set of Stackable 2mm patch chords -10 Nos.
- 4 User Manual.

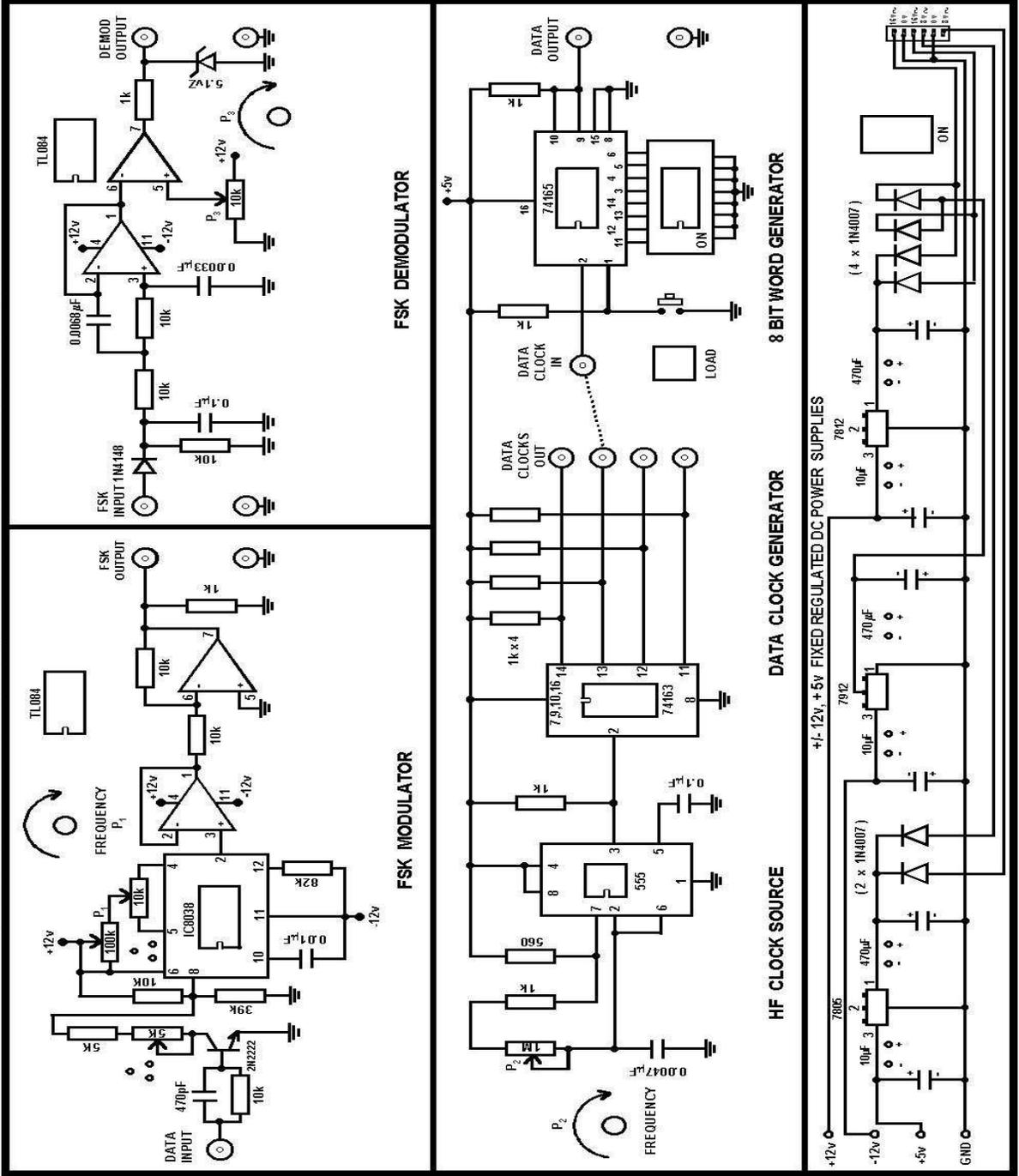
COMPONENT LIST

Description	Qty	Description	Qty
ICs		Diodes	
TL084	2 Nos	5.1v Zener	1 No
8038	1 No	1N4148	1 No
74163	1 No	1N4007	6 Nos
74165	1 No		
555	1 No	Potential Meters	
		100k Ω Linear 1 W	1 No
Resistors		10k Ω Linear 1W	1 No
560 Ω 1/2w 5% Tolerance	1 Nos	1M Ω Linear 1W	1 No
1k Ω 1/2w 5% Tolerance	10 Nos		
5k Ω 1/2w 5% Tolerance	1 No	Presets	
10k 1/2w 5% Tolerance	7 No	5k Ω	1 No
39k 1/2w 5% Tolerance	1 No		
82K 1/2w 5% Tolerance	1 No	Transistors	
		2N 2222	1 No
Capacitors		Regulators	
470pf	1 No	7812 To- 220 Package	1 No
0.01 μ f	1 No	7912 To-220 Package	1 No
0.1 μ f	2 Nos	7805 To- 220 Package	1 No
0.0068 μ f	1 No		
0.0033 μ f	1 No	Switch	
0.0047 μ f	1 No	DPST Switch(illuminated)	1 No
470 μ f /63v	3 Nos	DIP Switch 16 Pin	1 No
10 μ f /63v	3 Nos	Tactile Switch	1 No



**WAVE FORMS OF FREQUENCY SHIFT KEY
MODULATION & DEMODULATION**

FT 1556 FREQUENCY SHIFT KEYING MODULATION AND DEMODULATION



FUTURE TECH

PANEL LAYOUT DIAGRAM