

FACULTY PROFILE

1. Name : CH JAYAPRAKASH
2. Designation : ASSISTANT PROFESSOR
3. Department :ECE
4. Date of Joining :14/051/2011
5. Nature of Employment:Regular
6. Date of Birth : 10 MARCH 1983
7. Unique ID (AICTE FID) : 1-718038351
8. Email : jp.chennoju@sircrrengg.ac.in
9. Phone : 9441310177
10. Address for communication:2-138 , RTC PETA , NEAR SIDHARTHA SCHOOL,
SATRAM PADU, ELURU



11. Educational Qualifications:

Qualification	Institute	University/ Board	Specialization	Year of Passing	Division/ Class
Ph.D.	KLU	DEEMED	MEMS	PERSUING	-
PG	NOVA COLLEGE OF ENGG	JNTUK	VLSI SYSTEM DESIGN	2010	FIRST
UG	SREE KAVITHA ENGG COLLEGE	JNTUH	ECE	2006	FIRST
Inter/Diploma	KRANTHI JUNIOR COLLGE	BIE	MPC	2001	DISTINCTION
SSC	NIRMAL HRUDAI HIGH SCHOOL	SSC	EM	1999	FIRST

12. Work Experience:

Teaching: Research: Industry: Total:13

Name of the Organization	Designation	Date From	Date To
SAI SPURTHI INSTITUTE OF TECH	ASSISTANT PROFESSOR	26/05/2008	11/5/2010
SIR CRREDDY COLLEGE OF ENGG	ASSISTANT PROFESSOR	14/05/2011	TILL DATE

13. Courses taught:

S.No.	Name of the subject	UG/PG
1	ELECTRONIC DEVICES AND CIRCUITS	UG
2	ELECTRONICS CIRCUIT ANALYSIS	UG
3	SWITCHING THEORY AND LOGIC CIRCUITS	UG
4	LINEAR IC APPLICATION	UG
5	DIGITAL IC APPLICATION	UG
6	PULSE AND DIGITAL CIRCUITS	UG
7	MICRO PROCESSOR AND MICRO	UG

	CONTROLLERS	
8	SIGNALS AND SYSTEM	UG
9	DIGITAL LOGIC DESIGN	UG
10	MEMS	PG
11	DSDT	PG

14. Administrative Responsibilities:

S.No.	Description	College/ Department level
1	INTERNAL EXAM INCHARGE	Department level
2	JNTUK ONLINE MARKS INCHARGE	Department level
3	VLSI LAB INCHARGE	Department level
4	FEED BACK INCHARGE	Department level
5	COUNSELLING	Department level

15. Research Guidance:

M.Tech.		Ph.D.	
Completed	Ongoing	Completed	Ongoing
5	-	-	-

16. Research Publications in Journals (National/International):

S. No.	Author(s) Name	Title of the Paper	Name of the Journal	National/ International	Month & Year	Volume, Issue No, Page Nos	UGC/ Web of Science/ Scopus/ SCI/Others
1	CH. Jaya Prakash and N. Siddaiah	Detection of volatile organic compounds using Mems based microcantilever: a review	ARPJN Journal of Engineering and Applied Sciences	International	January 2021	VOL. 16, NO. 1	(SCOPUS)
2	Ch JayaPrakash, Miranji Katta, R. Spandanalakhmi, M Narendra Kumar	Static and Dynamic Analysis of CNT Cantilever for NEMS based Application.	Journal of Computational and Theoretical Nanoscience (JCATN)	International	Feb 2019-20	Vol:17,2,1-6	SCOPUS
3	Ch Jaya Prakash, P.Hareesh, P Geetha	Concede Threshold Analysis for logic gate Designs	IJMTE	International	2018-19	Vol-8, Issue-X, October-2018, Pages-1861-1867, ISSN:2249-7455	UGC Approved
4	Ch	Comparative analysis	Jour of Adv	International	2018-19	Vol.	SCOPUS

	JayaPrakash M Narendra Kumar ,vamsi krishna Miranji Katta, R,	of lead-free piezoelectric material for Ultrasonic glucose sensing applications	Research in Dynamical & Control Systems, , , 2019	al	APRIL	11,2,1110-1116	
5	Ch Jayaprakash	Area & delay efficient design for parallel prefix finate field multiplier	International Journal of Management, Technology And Engineering	Internati onal	OCT 2018-19	Volume 8,10,2983-2988	Others
6	Ch.Jaya Prakash, Dr PHS Tejo murthy,sunitha	A soft error tolerance technique for combinational circuit using D FF Basedon selective Transistor Redundancy	IJRAR	Internation al	2018-19	VOL 6, ISSUE 2,473-477	others
7	Ch.Jaya Prakash, Dr PHS Tejo murthy,Raji	Floating-point butterfly architecture based on redundant number system and Fused-Dot-Product-Add unit	IJAERD(International Journal of Advance Engineering and Research Development)	Internation al	2017-18	VOL 4,11,60-66	Others
8	CH JAYA PRAKASH, M VISWESWAR A RAO	A study on design and implementation of a real time embedded system for multiple image processing applications.	IJRECE(International Journal Of Research In Electronics & Communication Engineering)	Internation al	Aug 2016	VOL4,4,1550-1553	Others
9	CH. JAYA PRAKASH U. APARNA DEVI	An Efficient and Enhanced Low Power ETI Encoder for Serial Communication Links	International journal of scientific engineering & technology Research (IJSETR)	Internation al	2015	VOL4,10,1800-1804	Others
10	CH JAYAPRAKASH K.N.U Maheswari	An advance4d & Low Power LBIST For Cryptographic Applications	IRD India, International Journal on Advanced Computer Engineering and Communication Technology (IJACECT)	Internation al	2015	VOL4,2,28-33	Others
11	CH JAYAPRAKASH, A MOHAN VAMSI KRISHNA	Design of low power scalable Digital Comparator using a parallel prefix tree	International conference on electrical, electronics & computer systems(ICEE Cs)	Internation al	2014	VOL2,8,24-27	Others
12	CH JAYAPRAKASH, T.PrudhviRaju	Design of FIR Filter using Fifth approximation adder	International journal technology Research in engineering (IJTRE)	Internation al	2014	VOL3,2,124-127	Others
13	CH. JAYAPRAKASH T. INDIRA	Design of low power and high performance pulse triggered flip flop using conditional pulse enhancement method	Interscience open access journal, International Journal of Electrical and Electronics	Internation al	2013	VOL3,2, 25-31	Others

			Engineering (IJEEE)				
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17. Research Papers in Conferences (National/International):NIL

S.No.	Author(s) Name	Title of the Paper	Name of the Conference/Journal	National/ International	Month & Year	Page Nos
1	Ch Jaya Prakash, P Bhavya Priya	Heart Disease Prediction Using Machine Learning	2nd NATIONAL CONFERENCE ON "ARTIFICIAL INTELLIGENCE & MACHINE LEARNING"-	National-	2021	31
2	Ch Jaya Prakash, P V R V Dheeraj,	Recognition Of Frauds On Credit Card Using Machine Learning	2nd NATIONAL CONFERENCE ON "ARTIFICIAL INTELLIGENCE & MACHINE LEARNING"	National	2021	31
3	Ch jayaprakash	Implementing of hamming code using verilog	ICACT 2019	International	2019	187

18. No of Books Published:NIL

S.No.	Author(s) Name	Title	Publisher	ISBN	Year of Publishing
-	-	-	-	-	-

19. Workshops/ FDPs/STTPs /etc., (Organised):

S.No.	Name of the Workshop/ FDP/STTP/ etc.,	Place	Period	
			From	To
1	One week workshop on "Advanced Vlsi Training On Xilinx FPGA Using Vivado Tools"	SIR CRREDDY COLLEGE OF ENGG, eluru	16/09/2019	21/09/2019
2	Guest lecture on real time application of signals n systems	SIR CRREDDY COLLEGE OF ENGG, eluru	6/09/2018	6/09/2018
3	Two day Workshop on "FPGA based system design using Verilog " during 6 ^h & 7 th October 2017	SIR CRREDDY COLLEGE OF ENGG, eluru	06/10/2017	07/10/2017
4	Two day Workshop on TWO Day Work Shop On IC Design Flow Using Mentor Graphics Tools	SIR CRREDDY COLLEGE OF ENGG, eluru	05/08/2016	06/08/2016

20. Workshops/ FDPs/STTPs/ etc., (Attended):

S.No.	Name of the Workshop/ FDP/STTP/ etc.,	Place	Period	
			From	To
1	Mission10X workshop	Khammam	20/01/2009	24/01/2009
2	AICTE/MHRD summer School on Application of ICT for Hardware Laboratory	IIT KHARAGPUR	17/05/2009	23/05/2009
3	EMBEDDED SYSTEM PROGRAMMING(DEVICE DRIVERS) organized by CDAC Hyd in collaboration with JNTU H	CDAC HYD	18/05/2010	28/05/2010
4	Digital signal processing oraganiged by Dept of EEE Under QIP Programee	IIT ROORKEE UTTARAKHAND	26/02/2011	02/03/2011
5	Recent advancements in VLSI Technology & Design using EDA Tools conducted by CoreEL Technologies in collaboration with JNTUK	JNTU KAKINADA	20/07/2016	24/06/2016
6	One week training programmeon "INSTRUCTIONAL DESIGN AND DELIVERY SYSTEM"	SIR CRR COLLEGE OF ENGG	04/10/2017	9/10/2017
7	AI For Everyone	Coursera	02-05-20	
8	Programming for Everybody (Getting Started with Python)	Coursera	04-05-20	
9	ARTIFICIAL INTELLIGENCE	SIR CRREDDY COLLEGE OF ENGG	22-05-2020	TO 26-05-2020
10	Opportunities & Challenges in Electronics & Allied Industries in India post COVID-19"	Institution's Innovation Council (IIC) Vivekanand Education Society's Institute of Technology	25-05-2020	TO 30-05-2020
11	IOT WITH ARTIFICIAL INTELLIGENCE	SIR CRREDDY COLLEGE OF ENGG	27-05-2020 TO	29-05-2020
12	TRENDS IN COMMUNICATION	SIR CRREDDY COLLEGE OF ENGG	26-05-2020 TO	30-05-2020
13	AN EMERGING PARADIGM OF LOW POWER COMPUTATIONAL VLSI DESIGN	B V RAJU INSTITUTE OF TECHNOLOGY	16-06-2020	TO 20-06-2020

21. Sponsored Projects:NIL

S.No.	Title	Sponsored by	Amount	Period	Ongoing/ Completed
-	-	-	-	-	-

22. Consultancy Projects:NIL

S.No.	Title	Agency	Amount	Period	Ongoing/ Completed
-	-	-	-	-	-

23. No of Patents (Filed/Granted):NIL

S.No.	Title	Application Number	Year	Filed/Granted
-	-	-	-	-

24. Awards/HonoursReceived:NIL

S.No.	Award Name	Awarded by	Contribution	Date Received
-	-	-	-	-

25. Professional Memberships:

S.No.	Name of the Professional Body	Membership No.	Membership Type
1	LMISTE	LM59343	LIFE
2	MIETE	M-500571	LIFE
3	IAENG	135400	LIFE

26. Membership in BOS/ Editorial Boards:NIL

S.No.	Name of the University/ Journal	Member/ Editor/ Reviewer	Period
-	-	-	-

27. Details of Personal Blogs/ Educational Youtube Channels/ e content (if any):

Blog: <https://ecelegend.blogspot.com/>

youtube class links::

SUBJECT: ECA:R1922041 ::

<https://www.youtube.com/watch?v=hAqGHezoV4s&list=PLyVwY7dGCgsaZ69N00BmXGjREalqEID9g>

SUBJECT: STLD:R1921043:

https://www.youtube.com/watch?v=4bCvOGtSXLE&list=PLyVwY7dGCgsaBU2gdo5_0iGlmeuMW8o3t&index=17

EDMODO CLASS:

ECA:<https://new.edmodo.com/groups/eca-jp-37493063>

STLD-A:<https://new.edmodo.com/groups/stld-a-36292213>

STLD-B:<https://new.edmodo.com/groups/stld-b-36092520>

28. Details of Innovative Design/ Development of Product or Model (if any):NIL

29. Technology Transfer: NIL

30. Special Achievements (If any):NIL

31. Personal Details:

(a) Father's Name	: CH SATYA NARAYANA
(b) Mother's Name	: VIJAYALAKSHMI
(c) Gender	: MALE
(d) Marital Status	: MARRIED
(e) Religion	:HINDU
(f) Nationality	: INDIAN



Signature