FACULTY PROFILE

1. **Name :P.Hareesh**
2. **Designation : Assistant professor**
3. **Department :E.C.E Department**
4. **Date of Joining : 06-09-2010.**
5. **Nature of Employment:Regular**
6. **Date of Birth : 17-08-1987.**
7. **Unique ID (AICTE FID) : 1-435604814**
8. **Email : hareeshpancheti@gmail.com**
9. **Phone : 9030744615,9618496159**
10. **Address for communication: H.No:25-9-25, Old Post Office Street, N.R. Peta, Eluru, W.G.Dist., Andhra Pradesh-534006.**

11. Educational Qualifications:

Qualification	Institute	University/ Board	Specialization	Year of Passing	Division/ Class
Ph.D. (Ongoing)	Annamali University	Annamali University	E.C.E-MEMS		
PG	SASTRA University	SASTRA University	ECE-VLSI design	2010	First.
UG	Rao & Naidu Engineering College	JNTUH	E.C.E	2008	Second
Inter/Diploma	Montessori Jr. College	BoIE	MPC	2004	First
SSC	St.Arnolds High School	SSC	SSC	2002	First

12. Work Experience:

Teaching:11 Years 3 Months**Research:**Nil**Industry:**Nil.**Total:**11 Years 3 Months

Name of the Organization	Designation	Date From	Date To
Sir C.R Reddy College of Engineering	Assistant Professor	06-09-2010	Till date
Narasaraopeta Engineering College	Assistant Professor	02-06-2010.	02-09-2010.

13. Courses taught:

S.No.	Name of the subject	UG/PG
1	System design through Verilog	UG
2	VLSI Design	UG
3	VLSI Design & Embedded system	UG
4	Probability theory & Random process	UG
5	Electronics Measurements and Instrumentation	UG
6	Radar Engineering and Navigational Aids	UG

7	Signals and Systems	UG
8	Digital Signal Processing	UG
9	Managerial Economics and Financial Analysis	UG
10	Management Science	UG
11	History of Science and Technology	UG
12	Digital System Design using HDL (ongoing)	UG
13	Digital Signal Processing	PG
14	VLSI Design	PG
15	VLSI design techniques.	PG
16	VHDL Modelling of digital systems.	PG
17	Low Power VLSI Design	PG
18	CMOS Analog IC Design	PG
19	System on Chip Design	PG

14. Administrative Responsibilities:

S.No.	Description	College/ Department level
1	Department Furniture &Maintenance In charge	Department level
2	IETE Faculty Co-Ordinator	Department level
3	MoU's Incharge	Department level
4	Admission	College level

15. Research Guidance:

M.Tech.		Ph.D.	
Completed	**Ongoing**	**Completed**	**Ongoing**
Completed			Ongoing

16. Research Publications in Journals (National/International):

S.No.	Author(s) Name	Title of the Paper	Name of the Journal	National/ International	Month & Year	Volume, Issue No, Page Nos	UGC/ Web of Sciences/ Scopus/ SCI/Others
1.	K. Hari Krishna, P. Hareesh,	A New Low Power Technology for Power Reduction in SRAM's Using Read Stability with Reduced Transistor Count for Future Catches	IJESS	International	2013	Vol-3,pp. 88-91, ISS-2,2013,ISSN :2231-5969.	Others
2.	G. Lakshmi Praeetha, P. Hareesh	"STDFF A Pass Transistor Based Flip-Flop Design for Efficient Integrated Circuits"	IJESS	International	2013	Vol-3, pp. 114-117, ISS-2, 2013, ISSN: 2231-5969.	Others
3.	P.Hareesh, K. Harikrishna, G. Lakshmi Praneetha,	"MTCMOS Full Subtractor With Low Power Consumption and Reduced Leakage	IJECT	International	2014	IMPACT Factor: 1.319 (2015) International	Others

		power"				Scientific Indexing. Vol.5, pp.71-73, Issue Spl-3, Jan-March 2014, ISSN: 2230-7109(Online), ISSN: 2230-9543(Print).	
4.	P. Hareesh, R.Trinadh, V.Krishnan,G.N.Murthy	Exploiting Rising and Charge-Sharing Voltage for Power Management in High Speed Domino Circuits	IJECT	International	2014	IMPACT Factor: 1.319 (2015) International Scientific Indexing. Vol.5, pp.77-80, Issue Spl-3, Jan-March 2014, ISSN: 2230-7109(Online), ISSN: 2230-9543(Print).	Others
5.	M.Greeshma, P.Hareesh	Design Low-Power Pulse-Triggered Flip-Flop design based on a Signal Feed-Through Scheme	IJEECS	International	2014	IMPACT Factor: 2.04 Vol.2, pp.28-31, Issue-8, 9, 2014, ISSN: 2347-2820(Online).	Others
6	Anupama.Ch, P.Hareesh	A Digital CMOS Parallel Counter Architecture	IJEECS	International	2014	IMPACT Factor: 2.04 Vol.2, pp.38-42, Issue-8, 9 2014, ISSN: 2347-2820(Online).	Others
7	Sk.Abdual Kadar, P.Hareesh	Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Using Power Gating Techniques	IJMETMR	International	2015	IMPACT Factor: 1.7450 (2015) International Journal Impact Factor. ISSN No: 2320-3706(Print) ISSN No: 2348-4845(Online).	Others
8	Ch.Salini, P.Hareesh	Latency Optimized Square and Cube Architecture using Vedic Sutras	IJSETR	International	June-2015	IMPACT Factor: 4.162 Vol.04, Issue No.19, June-2015, ISSN 2319-8885.	Others
9	P.Venkatesh, P. Hareesh	Hardware Implementation of Digital Watermarking	IJITECH	International	August-2016	IMPACT Factor: 3.864 ISSN 2321-	Others

		System for Real Time Captured Image Transmitting				8665 Vol.04,Issue.10 , August-2016, Pages:1733-1736	
10	A. Suresh Babu, P. Hareesh	Design and implementation of Brent Kung carry select adder using pass transistor logic techniques	IJRECE	International	March-April, 2016	Vol–4, Issue-3. Mar - Apr, 2016, ISSN:2321-5593(Online) ISSN: 2321-032X(Print)	Others
11	P.Hareesh, S V Abhishek	Design of DPLL and Implementation of BIST to Evaluate its Characteristics	IJAERD	International	November -2017-18	Vol-04,issue 11, November - 2017, e-ISSN: 2348-4470,p-ISSN: 2348-6406	UGC Approved
12	P.Gopi Krishna, K.Srinivasa R P.Hareesh, D.Ajay Kumar, H.Sudhakar	Implementation of Bi-Directional Blue-Fi Gate Way in IOT Environment	IJET	International	2017-18	Vol-07, Special issue 8,2018,pages -97-102 ISSN: 2227-524X	Scopus
13	P.Hareesh, Ch Jaya Prakash, P Geetha	Concede Threshold Analysis for logic gate Designs	IJMTE	International	2018-19	Vol-8,Issuse-X,October-2018, Pages-1861-1867, ISSN:2249-7455	UGC Approved
14	Ch Jaya Prakash, P.Hareesh,Sk. Farishma	Area and delay efficient design for parallel Prefix finite field multiplier	IJMTE	International	2018-19	Vol-8,Issuse-X,October-2018, Pages-2983-2988 ISSN:2249-7455	UGC Approved

17. Research Papers in Conferences (National/International):

S.No.	Author(s) Name	Title of the Paper	Name of the Conference/Journal	National/ International	Month & Year	Page Nos
1	P. Hareesh, A. Uma maheshwara reddy	Modified High Speed Vedic Multiplier Implementation Using	2nd NATIONAL CONFERENCE ON "ARTIFICIAL INTELLIGENCE & MACHINE LEARNING"	national	2021	28

		VLSI				
2	P.Hareesh	Ardino based gesture to speech conversion for the mute comunity	ICACT 2019	international	2019	212
1.	K.Hari Krishna, P.Hareesh	A Novel Power Reduction Technology in SRAM's using Read Stability with Reduced Transistor Count for Future Caches for Low Power Applications	ICRTST-RTET	International	29th September 2013	119-122
2.	G.LakshmiPraneetha, P.Hareesh	An Efficient Integrated Circuit Design For a Pass Transistor D Flip-Flop (STDFF)	ICRTST-RTET	International	29th September 2013	60-63

18. No of Books Published:

S.No.	Author(s) Name	Title	Publisher	ISBN	Year of Publishing
	Nil				

19. Workshops/ FDPs/STTPs /etc., (Organised):

S.No.	Name of the Workshop/ FDP/STTP/ etc.,	Place	Period	
			From	To
1.	Guest lecture on "startups and latest technology awareness"	SIR CRRCOE,Eluru	20-12-2020	20-12-2020

20. Workshops/ FDPs/STTPs/ etc., (Attended):

S.No.	Name of the Workshop/ FDP/STTP/ etc.,	Place	Period	
			From	To
1.	"Analog& Digital VLSI Circuits Design" using Cadence EDA Tools	Dept. of E.C.E, ACE Engineering College, Ankushapur(V), Gatkesar(M), R.R. Dist., A.P, India.	27-06-2011	29-06-2011
2.	"Analog, Digital and Mixed Signal VLSI Design",	Dept. of E.C.E, Gudlavalleru Engineering College, Seshadri Rao Knowledge Village, Gudlavalleru, Krishna Dist., A.P, India	15-10-2011	--
3	"VLSI Design"	School of Electronics, Vignan University, Vadlamudi, Guntur Dist., A.P, India.	06-02-2012	07-02-2012
4	"PLC Programming & Applications"	Sir C R Reddy College of Engineering, Eluru, W.G (D.T),A.P,India.	01-03-2015	--
5	"Recent Advancements in VLSI Technology and Design Using EDA Tools(VLSITP-2016)"	JNTU,UCOEK(A), Kakinada,A.P,India.	20-07-2016.	24-07-2016
6	"IC Design Flow using Mentor Graphics EDA tools"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	05-08-2016	06-08-2016
7.	"3D Modelling of Electromagnatic Systems Using ANSYS RF-Tools"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	09-09-2016.	10-09-2016
8.	"FPGA based system design using Verilog"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	06-10-2017	07-10-2017
9.	"CMOS Analog IC Design"	V R Siddharth Engineering College,Vijayawada, Krishna(D.T),A.P., India.	13-11-2017	18-11-2017
10.	"Introduction to Research"	NPTEL-IITM		

21. Sponsored Projects:

S.No.	Title	Sponsored by	Amount	Period	Ongoing/ Completed
	Nil				

22. Consultancy Projects:

S.No.	Title	Agency	Amount	Period	Ongoing/ Completed
	Nil				

23. No of Patents (Filed/Granted):

S.No.	Title	Application Number	Year	Filed/Granted
	Nil			

24. Awards/HonoursReceived:

S.No.	Award Name	Awarded by	Contribution	Date Received
	Nil			

25. Professional Memberships:

S.No.	Name of the Professional Body	Membership No.	Membership Type
1	MIE	AM163845-1	Associate
2	IETE	AM-500605	Associate
3	IAENG	135737	Permanent Member

26. Membership in BOS/ Editorial Boards:

S.No.	Name of the University/ Journal	Member/ Editor/ Reviewer	Period
	NIL		

27. Details of Personal Blogs/ Educational Youtube Channels/ *e* content (if any):

https://hareeshpancheti.blogspot.com

28. Details of Innovative Design/ Development of Product or Model (if any):

nil

29. Technology Transfer:

30. Special Achievements (If any):

- **Ratified as Assistant Professor from Andhra University**
- **Ratified as Assistant Professor from JNT University, Kakinada.**

31. Personal Details:

(a) Father's Name : P.Venkateswarlu (late)

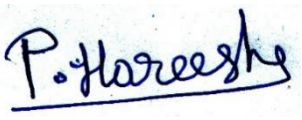
(b) Mother's Name :P.Sujatha

(c) Gender : male

(d) Marital Status : married

(e) Religion : Hindu.

(f) Nationality : Indian



Signature