II B. Tech I Semester Regular/Supplementary Examinations, October/November - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Com to ECE, EIE and ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert the following numbers with the given radix to decimal. (2M)
   i. 61_7 ii. $A1_{16}$
   b) Prove that NAND gates are universal gates. (3M)
   c) Define Decoder? List out the applications of it? (3M)
   d) Draw the basic architecture of a PAL? (2M)
   e) Give the Excitation table for J-K Flip-flop (2M)
   f) Compare Melay and Moore models (2M)

PART -B

2. a) Perform the subtraction using 1's complement and 2's complement methods. (8M)
   (i)11010 – 10011 (ii)11000 – 1011 (iii)111 - 110000
   b) A 7 bit Hamming code is received as 1110101.Is there any error? If yes, locate the position of the error bit. Parity checks are created by odd parity. (6M)

3. a) Reduce the following function using k-map technique F(A,B,C,D)=ΠM(1,2,3,5,6,7,8,9,12,13) . (7M)
   b) Design a combinational circuit that converts four bit binary number into gray code (7M)

4. a) Perform the realization of full subtractor and full adder using decoders and logic gates (6M)
   b) Realize the function f(A,B,C,D) = ∑ (1,2,5,6,7,8,10,14,15) using (8M)
   i) 8:1 MUX ii) 4:1 MUX

5. a) Discuss how PROM, EPROM and EEPROM technologies differ from each other. (6M)
   b) Realize the following four Boolean functions using PAL. (8M)
   F1(w,x,y,z) = ∑m(1,2,3,7,9,11) F2(w,x,y,z) = ∑m(0,1,2,3,10,12,14)
   F3(w,x,y,z) = ∑m(4,5,6,7,9,15) F4(w,x,y,z)=∑m(1,2,3,10,13,15)

6. a) Convert T flip-flop into D and JK flip-flops (6M)
   b) Design a mod-12 Ripple counter using T flip flops and explain its operation. (8M)

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7. a) Draw the diagram of Mealy type FSM for serial adder. (7M)

b) Find the equivalence partition and a corresponding reduced machine in a standard form for a given machine. (7M)

PS	NS , Z	
	X=0	X=1
A	C,1	E,1
B	A,0	D,1
C	E,0	D,1
D	F,1	A,1
E	B,1	F,0
F	B,1	C,1

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PART –A

1\. a) Convert the following numbers with the given radix to decimal. (2M)
i. 61_8 ii. $B2_{16}$

b) Prove that NOR gates are universal gates. (3M)

c) Define Multiplexer? (2M)

d) Draw the basic architecture of a PLA? (2M)

e) Give the Excitation table for R-S Flip-flop (2M)

f) Distinguish between synchronous and asynchronous machines. (3M)

PART -B

2\. a) Determine the canonical sum-of-products representation of the following functions (7M)
i) f(A,B,C) =C+ ($\bar{A}$+B)(A+$\bar{B}$)
ii) f(A,B,C) =A +($\overline{\bar{A}\bar{B} + \bar{A}C}$)

b) Given the 8bit data word 01001001, generate the 12 bit composite word for the hamming code that corrects and detects single error (7M)

3\. a) Reduce using mapping the following expression and implement the real minimal expression using logic gates. (7M)
f(A,B,C,D)= ∏M (1,3, 5, 9, 11, 14)

b) Using the Quine–McCluskey tabular method, find the minimum sum of products for (7M)
F(A,B,C,D,E) =∑m(1,5,6,7,9,13,14,15,17,18,19,21,22,23,25,29,30)

4\. a) Design a excess-3 adder using 4-bit parallel binary adder and logic gates. (7M)

b) Construct a 4x16 decoder using logic gates and explain its operation with the help of truth table. (7M)

5\. a) Design a BCD to Excess-3 code converter using a PROM (7M)

b) Give the comparison between PROM,PLA and PAL (7M)
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6. a) Design a SR flip flop using NAND gates. Explain the operation of the SR flip flop with the help of characteristic table and characteristic equation. (7M)
   b) Explain the operation of 4-bit ring counter with circuit diagram and timing diagrams. (7M)

7. a) Write the differences between Mealy and Moore type machines (7M)
   b) Convert the following Moore machine into a corresponding Mealy Machine (7M)

PS	NS		Z
	X=0	X=1	
A	D	B	1
B	A	E	0
C	A	E	1
D	C	A	0
E	F	D	0
F	F	D	1

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PART –A

1. a) Convert the following numbers with the given radix to decimal. (2M)
i. 52_7 ii. $C2_{16}$
b) Reduce the following Boolean expression using Boolean theorems. (2M)
ab+$\bar{a}$b+$\bar{a}\bar{b}$c+....
c) Define priority encoder? (2M)
d) Realize the two input X-NOR gate using minimum number of NOR gates. (3M)
e) Draw the state diagram for S-R & T Flip-Flop . (3M)
f) What is the principal advantage of a PLD? (2M)

PART -B

2. a) Determine the canonical product-of-sums representation of the following functions (7M)
i) f(A,B,C) =C ($\bar{A}$+B)(A+$\bar{B}$)
ii) f(A,B,C) =A($\overline{\bar{A}\bar{B} + \bar{A}C}$)
b) Perform the subtraction using 1's complement and 2's complement methods. (7M)
(i)11010 – 10111 (ii)11000 – 1010 (iii)1110 - 110000

3. a) Reduce using mapping the following expression and implement the real minimal expression using logic gates. (7M)
f(A,B,C,D)= ∑m (0,2, 4, 6,7,9, 11, 14)
b) Using the Quine–McCluskey tabular method, find the minimum sum of products for (7M)
F(A,B,C,D) =∑m(1,5,6,12,13,14)+∑d(2,4)

4. a) Design a BCD adder using 4-bit parallel binary adder and logic gates. (7M)
b) Realize the function f(A,B,C,D) = ∑ (1,3,4,6,7,8,10,13,15) using (7M)
i) 16:1 MUX ii) 8:1 MUX

5. a) Implement the following Boolean functions using PLA. (7M)
A(x,y,z)= ∑m(0,1,2,4,6)
B(x,y,z)= ∑m(0,2,6,7)
C(x,y,z)=∑m(3,6)
b) Design a Excess-3 to BCD code converter using a PROM (7M)

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6. a) Design a SR flip flop using AND gates and NOR gates. Explain the operation of the SR flip flop with the help of characteristic table and characteristic equation (7M)
   b) Explain the operation of 4-stage twisted ring counter with circuit diagram and timing diagram. (7M)

7. a) Draw the diagram of Mealy type FSM for serial adder (7M)
   b) Convert the following Mealy machine into a corresponding Moore Machine (7M)

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

Code No: R1621042 **R16** SET - 4

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PART –A

1. a) Convert the following numbers with the given radix to decimal. (2M)
i. 73_8 ii. $A4_{16}$
b) Reduce the following Boolean expression using Boolean theorems. (3M)
xy+$\bar{y}$ $\bar{z}$+wx$\bar{z}$
c) Realize Full subtractour using Half subtractors and logic gate (3M)
d) Realize the two input X-OR gate using minimum number of NAND gates. (2M)
e) Write the characteristic equations for S-R Flip-flop & T Flip-Flop. (2M)
f) What is meant by self correcting counters?. (2M)

PART -B

2. a) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation. (7M)
b) What is a Gray code? Obtain a 4-bit and 3-bit gray code from a 2-bit gray code by reflection. Explain its application in data converters. (7M)

3. a) Design a combinational circuit that converts four bit gray number into binary code (7M)
b) Simplify the following using tabulation method (7M)
F(A,B,C,D,E) = ∑m(0,4,12,16,19,24,27,28,29,31).

4. a) Construct the 4 bit parallel adder with look ahead carry generation. (7M)
b) Draw the logic diagram of a 3 to 8 line decoder with enable input and explain its operation with the help of truth table. (7M)

5. a) Design a BCD to Excess-3 code converter using a PROM (7M)
b) What is a PLD? Compare the three combinational PLDs? (7M)

6. a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation (7M)
b) What are the different types of registers? Explain the Parallel Input Serial Output shift register (7M)
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7. a) What are the Moore and Mealy machines? Compare them. (7M)

b) Reduce the number of states in the following state table and tabulate the reduced state table. (7M)

PS	NS,Z	
	X=0	X=1
A	A,0	E,1
B	E,1	A,0
C	F,1	B,0
D	B,0	F,1
E	C,1	C,0
F	G,0	C,1
G	H,0	D,1
H	D,1	H,0

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