

Code No: R164104C

R16

Set No. 1

IV B.Tech I Semester Regular Examinations, October/November - 2019

SYSTEM DESIGN THROUGH VERILOG

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

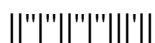
Answer any FOUR questions from Part-B

PART-A (14 Marks)

1. a) Compare Verilog and VHDL. [3]
- b) What is inertial delay? [2]
- c) Write the syntax for while loop. [3]
- d) How strength and delays are instantiated? [2]
- e) Differentiate synthesis and simulation. [2]
- f) Compare SRAM with DRAM. [2]

PART-B (4x14 = 56 Marks)

2. a) Explain about operators used in Verilog. [4]
- b) Define the following terms relevant to Verilog HDL:
(i) Parameters (ii) Strengths
(iii) Exercises (iv) Concurrency [10]
3. a) Design module and a test bench for conversion of an 8-bit number into its respective BCDs. [7]
- b) Write relevant syntax, logic diagrams and verilog code for Tristate gate. [7]
4. a) How are blocking assignments different from non blocking assignments? [7]
- b) Use the **disable** construct and prepare modules for AND, NAND and NOR functions. [7]
5. a) Write verilog code for CMOS switch and its test bench. [7]
- b) Implement the verilog HDL source code and logic diagram for 1-bit full adder using dataflow style. [7]
6. a) Write a verilog code for traffic light controller. [10]
- b) Write a verilog code for a latch. [4]
7. a) Discuss about read cycle timing of SRAM. [7]
- b) Design HDL model ALU operations for register memory instructions. [7]



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Set No. 2

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SYSTEM DESIGN THROUGH VERILOG

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Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any FOUR questions from Part-B

PART-A (14 Marks)

1. a) List out the different levels of design descriptions in verilog. [2]
- b) Mention all types of delays. [3]
- c) Write the syntax for Forever loop. [3]
- d) What is switch primitives? [2]
- e) What is net list? [2]
- f) What is UART? [2]

PART-B (4x14 = 56 Marks)

2. Define the following terms relevant to Verilog HDL
(i) Test bench (ii) Simulation tools
(ii) System tasks (iii) Level of design Description [14]
3. a) Draw the Half adder circuit in terms of Ex-OR gates and AND gates. Prepare a Half adder module in terms of Ex-OR gate and AND gate primitive. [7]
b) Explain in brief built-in primitive gates that are available in Verilog HDL. [7]
4. a) Write verilog code of an 8 bit counter. [7]
b) Use the **repeat** construct along with the **disable** construct to realize an AND gate. Synthesize the module and compare the synthesized circuits. [7]
5. a) Explain Bi-directional gates with suitable logic diagrams and give their verilog code using switch level modeling. [7]
b) Realize the skeletal edge-triggered flip flop through continuous assignments for the gates. Write its test bench. [7]
6. a) Discuss Moore machine using verilog. [10]
b) Write a verilog code for 8×1 MUX. [4]
7. Explain the modeling approach for static RAM memory using verilog HDL. Modeling approach consists of design and implementation. [14]



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Set No. 3

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SYSTEM DESIGN THROUGH VERILOG

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any FOUR questions from Part-B

PART-A (14 Marks)

1. a) What are the system tasks available in verilog for monitoring? [3]
- b) Classify delays. [2]
- c) Write the syntax for repeat construct. [2]
- d) Write verilog code for 2×1 MUX using CMOS [3]
- e) What is latch? [2]
- f) What is baud rate? [2]

PART-B (4x14 = 56 Marks)

2. a) Explain top-down design methodology with examples? [7]
- b) Define the following terms relevant to Verilog HDL:
(i) Keywords (ii) Identifiers
(iii) Strings (iv) Data types [7]
3. a) Explain NAND gate primitive with verilog module. [7]
- b) Implement verilog HDL source code and draw the logic diagram of a 2 to 4 decoder circuit. Give the gate level description. [7]
4. a) Describe the behavior of a JK flip flop using an **always** statement. [7]
- b) Prepare design modules and a test bench for the following operations:
(i) Add two BCD nibbles.
(ii) Add two pairs of BCD nibbles – 2 decimal numbers each of two digits. [7]
5. Implement NAND, AND, OR gates using MOS switches. Write verilog code and Test it with a suitable test bench. [14]
6. a) Explain the synthesis of sequential logic with flip flops. [7]
- b) What is continuous assignment statement? Explain with example. [7]
7. a) Explain the modeling approach for UART using verilog HDL. Modeling approach consists of design and implementation. [14]



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Set No. 4

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SYSTEM DESIGN THROUGH VERILOG

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any FOUR questions from Part-B

PART-A (14 Marks)

1. a) What are the different data types in verilog? [3]
- b) List out built-in primitive gates in verilog HDL. [2]
- c) Write the syntax for case statement. [3]
- d) Draw the CMOS switch. [2]
- e) Write a verilog code for a D-flip flop. [2]
- f) What are the different ALU operations? [2]

PART-B (4x14 = 56 Marks)

2. a) Define the following terms relevant to Verilog HDL:
(i) Verilog as HDL (ii) Functional verification
(iii) Module (iv) PLI [14]
3. a) Write a verilog code of a master slave flip-flop with gate primitives. [7]
- b) Give verilog syntax on gate delays with necessary instantiations. [7]
4. a) Write the difference between begin-end and fork-join blocks with an example. [7]
- b) Design verilog code of OR gate using **for** and **disable**. Write simulation results with explanation. [7]
5. a) Explain continuous assignment structures relevant to dataflow modeling with suitable examples. [7]
- b) Implement the verilog HDL module for a 4 to1 vector multiplexer circuit using dataflow level. [7]
6. a) Explain the synthesis process of explicit state machines. [7]
- b) Give the differences between accidental synthesis of latches and intentional synthesis of latches. [7]
7. Design HDL module for Baud rate generator. [14]

