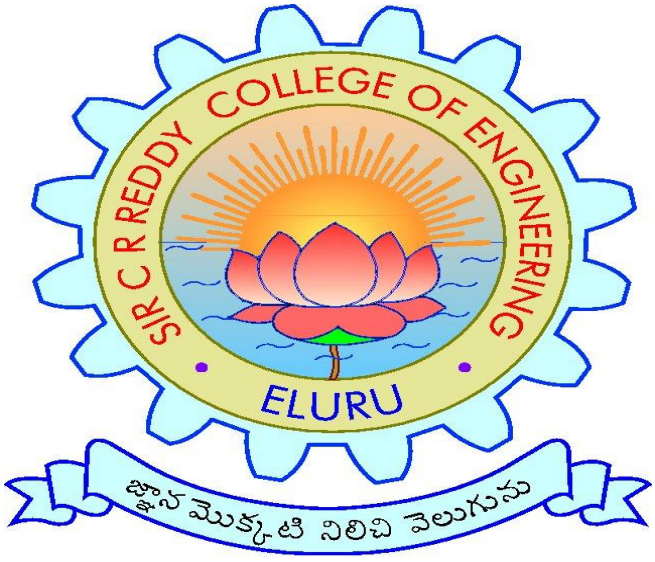
SIR C.R.REDDY COLLEGE OF ENGINEERING, ELURU

DEPARTMENT OF INFORMATION TECHNOLOGY

LESSON PLAN



SUBJECT: CSE 2.1.6 DIGITAL LOGIC DESIGN

CLASS: 2/4 B.Tech., I SEMESTER, A.Y.2017-18

INSTRUCTOR: Sri A.M.K.KANNA BABU

SIR C R REDDY COLLEGE OF ENGINEERING
DEPT. OF INFORMATION TECHNOLOGY

PROGRAMME : B.Tech
SEMESTER : II/IV I Semester
A.YEAR : 2017-18

COURSE : CSE 2.1.6 DIGITAL LOGIC DESIGN

INSTRUCTOR : Sri A.M.K.KANNA BABU

Course Contents

Category of Course	Course Title	Course Code	Credits- 4	Theory Paper
Departmental Core - CSE 2.1.6	DIGITAL LOGIC DESIGN	CSE 2.1.6	L-3 T-1	Max.Marks-70 Duration-3hrs.

Course objectives:

1. To introduce number systems and Binary codes.
2. To introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions and Boolean functions.
3. To introduce the methods for simplifying Boolean expressions.
4. To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits.
5. To introduce the concept of memories, programmable logic devices.

Students who have successfully completed this course will have full understanding of the following concepts

Course Outcomes for Digital Logic Design:

- Able to understand Binary Systems, Boolean Functions, Logic Gates, Combinational Circuits, Sequential Circuits and different types of memories.
- Able to apply number systems, Boolean functions and logic gates for the design of digital circuits.
- Able to analyze different logic circuits (like combinational and sequential circuits).
- Able to design different digital circuits.

Online References:

www.electronics-tutorials.ws
https://www.cse.iitb.ac.in/~supratik/courses/cs226

Prerequisite:

Students are expected to know mathematical fundamental and logical skills.

Internal Assessment Details:

Attendance	: 5 Marks
Internal Test 1& 2	: 15 Marks
Assignment-1	: 5 Marks
Assignment-2	: 5 Marks
Total	: 30 Marks

DIGITAL LOGIC DESIGN

CSE2.1.6 **Credits : 4**

Instruction : 3 Periods & 1 Tut /week **Sessional Marks : 30**

University-Exam : 3 Hours **Univ-Exam Marks:70**

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1. **Binary Systems:**
   Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Binary Numbers. Binary Codes. Binary Storage and Registers. Binary Logic.

2. **Boolean algebra and Logic Gates.**
   Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits.

3. **Combinational Logic Design, Gate-Level Minimization.**
   The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't-Care Conditions. NAND and NOR Implementation. Other Two-Level Implementations. Exclusive-OR Function. Hardware Description Language (HDL).

4. **Combinational Logic**
   Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers. HDL For Combinational Circuits.

5. **Sequential Logic Design, Synchronous Sequential Logic**
   Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits. HDL For Sequential Circuits. State Reduction and Assignment. Design Procedure.

6. **Registers ad Counters.**
   Registers. Shift Registers. Ripple Counters. Synchronous Counters. Other Counters. HDL for Registers and Counters.

7. **Memory and Programmable Logic**
   Introduction. Random-Access Memory. Memory Decoding. Error Detection and Correction. Read-Only Memory. Programmable Logic Array. Programmable Array Logic. Sequential Programmable Devices.

Text Books:

1. Digital Design, 3rd Edition, M. Morris Mano, Pearson Education, Inc., 2002

SIR C R REDDY COLLEGE OF ENGINEERING: ELURU

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE SCHEDULE

The schedule for the whole course/subject is:

Unit No	Description of the Chapter	Description of the Topics	Total no of periods (L+T)
1	Binary Systems	Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Binary Numbers. Binary Codes. Binary Storage and Registers. Binary Logic.	14+1
2	Boolean algebra and Logic Gates	Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits.	10
3	Combinational Logic Design, Gate-Level Minimization	The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't-Care Conditions. NAND and NOR Implementation. Other Two- Level Implementations. Exclusive-OR Function. Hardware Description Language (HDL).	9+1
4	Combinational Logic	Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder- Subtractor. Decimal Adder. Binary Multiplier. Magnitude Comparator. Decoders. Encoders.	9+1

		Multiplexers. HDL For Combinational Circuits.	
5	Sequential Logic Design, Synchronous Sequential Logic	Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits. HDL For Sequential Circuits. State Reduction and Assignment. Design Procedure.	9+1
6.	Registers and Counters.	Registers. Shift Registers. Ripple Counters. Synchronous Counters. Other Counters. HDL for Registers and Counters.	5
7.	Memory and Programmable Logic	Introduction. Random-Access Memory. Memory Decoding. Error Detection and Correction. Read-Only Memory. Programmable Logic Array. Programmable Array Logic. Sequential Programmable Devices.	4+1

Total number of estimated periods : 65 periods

Signature of the H.O.D

Signature of the Faculty

Date:

	LECTURE PLAN
DEPARTMET	INFORMATION TECHNOLOGY
NAME OF LECTURER	Sri A.M.K.KANNA BABU

Sl. No	**Topics to be covered**	**No. of Lecture**	**Teaching method**
1	Introduction to Digital Systems	1	BB
2	Binary numbers	1	BB
3	Number system conversion	2	BB
4	Octal and Hexadecimal Numbers	1	BB
5	Complements	2	BB
6	Signed Binary Numbers	2	BB
7	Binary Codes	2	BB
8	Binary Storage and Registers	2	PPT with LCD
9	Binary Logic	2	BB
10	Basic Definitions	1	BB
11	Axiomatic Definition of Boolean Algebra	1	BB
12	Basic Theorems and Properties of Boolean Algebra	1	BB
13	Boolean Functions	1	
14	Canonical and Standard Forms	2	BB

15	Other Logic Operations	2	BB
16	Digital Logic Gates	1	BB
17	Integrated Circuits	1	BB
18	The Map Method	1	PPT with LCD
19	Four-Variable Map	1	BB
20	Five-Variable Map	2	BB
21	Product of Sums Simplification	1	BB
22	Don't-Care Conditions	1	BB
23	NAND and NOR Implementation	1	
24	Other Two- Level Implementations	1	BB
25	Exclusive-OR Function	1	BB
26	Hardware Description Language (HDL)	1	BB
27	Combinational Circuits Analysis Procedure	1	BB
28	Design Procedure	1	BB
29	Binary Adder- Subtractor	1	PPT with LCD
30	Decimal Adder	1	
31	Binary Multiplier	1	BB
32	Magnitude Comparator	1	BB
33	Decoders	1	BB

34	Encoders	1	BB
35	Multiplexers	1	
36	HDL For Combinational Circuits	1	BB
37	Sequential Circuits	1	BB
38	Latches	1	BB
39	Flip-Flops	2	BB
40	Analysis of Clocked Sequential Circuits	2	BB
41	HDL For Sequential Circuits	1	BB
42	State Reduction and Assignment	1	BB
43	Design Procedure	2	BB
44	Registers	2	BB
45	Counters	3	BB
46	Introduction Memory RAM and ROM	1	BB
47	Error Detection and Correction	1	BB
48	Programmable Logic Array	1	BB
49	Programmable Array Logic	1	PPT with LCD
50	Sequential Programmable Devices	1	BB

Total number of estimated periods : 65 periods

Unit wise questions (short and essay)
DIGITAL LOGIC DESIGN

Unit Wise Question Bank

UNIT-I

1. Find the two's complements of following numbers:

   a) $(1230)_4$ and $(23)_4$
   b) $(135.4)_6$ and $(43.2)_6$

2. Convert the following numbers from the given base to the base indicated.

   a) decimal 225.225 to binary, octal and hexadecimal.
   b) Binary (11010111.110) to decimal, octal and hexadecimal;

3. Convert the following numbers from the given base to the base indicated.

   a) octal 623.77 to decimal, binary and hexadecimal

   b) hexadecimal 2ACD.5 to decimal, binary and octal.

4. Convert the following number to decimal

   a) $(0.342)_6$ b) $(8.3)_9$
   c) $(198)_{12}$ d) $(50)_7$

5. Obtain the 9's and 10's complement of the following decimal numbers

   a) 13579

   b) 09900

   c) 10000

   d) 00000

   e) 90090

6. Obtain the 1's and 2's complement of the following binary numbers

   a) 1010101
   b) 0111000
   c) 0000001
   d) 10000
   e) 00000

7. Perform the subtraction with the following numbers using 2's and 1's complement

   a) 11010.1101 – 10010.10011
   b) 11010.10000 – 100.110000

8. Explain

a) self-complementary codes with examples.

b) Error-detection codes and Reflected Code

9. Explain

a) BCD codes
b) Register transfer with a neat diagram.

10. a) Explain basic logic gates with a truth tables and gates

b) Define Boolean algebra and prove the following theorems

(i) X + X = X

(ii) X.0 = 0

(iii) X + XY = X

(iv) $(XY)^1 = X^{1+}Y^1$

UNIT-II

1. Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer.

   (Use only block diagram).

2. A combinational logic circuit is defined by the following Boolean functions.

   F1 = ABC + AC

   F2 = ABC + AB

   F3 = ABC + AB

   Design the circuit with a decoder and external gates. xy + x (wz + wz').

3. If F1 = Π 3,4,7,8,11,14,15 and F2 = Σ1,2,4,5,7,8,10,11,12,15 obtain minimal SOP expression for F1 • F 2 and draw the circuit using NAND gates.

4. Draw the two -level NAND circuit for the following Boolean - expression:

   AB + CD E + BC (A + B) also obtain minimal SOP expression and draw the circuit using NAND gates.

5. If F1(A,B,C) = A _ B _ C

   F2 (A,B,C) = A_C _B Show that F1 = F2

6. Construct K-map for the following expression and obtain minimal SOP expression.

   Implement the function with 2-level NAND -NAND form.

   f (A,B,C,D) = (A + C + D) (A + B + D)(A + B + C^1)(A + B + D)(A^1 + B + D)

7. Implement the following Boolean function F using the two - level form:

   i. NAND-AND

   ii. AND-NOR F (A,B,C,D) = _0, 1, 2, 3, 4, 8, 9, 12

UNIT-III

1. What is a flip-flop?

2. What is a latch?

3. What is a sequential circuit?

4. What is asynchronous sequential circuit?

5. Draw and explain the logic diagram of a master-slave D flip-flop using NAND gates.

6. a) Design a synchronous BCD counter with JK flip-flops.

   b) Design a shift register with parallel load that operates according to the following function table:

Shift	Load	Register Operation
0	0	No Change
0	1	Load Parallel Data
1	X	Shift Right

7. (a) Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.

(b) Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram.

8. Reduce the number of states in the state table listed below. Use an implication table.

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	0	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

UNIT-IV

1. What is a RAM?

2. Explain types of RAM?

3. What is a ROM?

4. Explain types of ROM?

5. What is a PAL?

6. What is a PLA?

7. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.

(b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.

ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?

iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder.

8. Explain RAM and ROM?

9. Explain PAL?

10. Explain PLA?