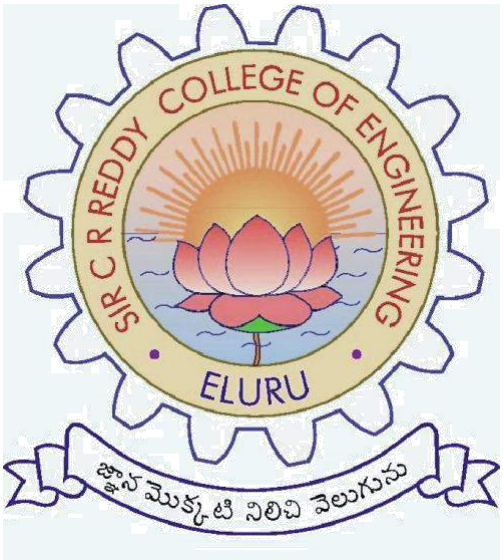
SIR C.R.REDDY COLLEGE OF ENGINEERING ELURU – 534 007

DIGITAL INTEGRATED CIRCUITS (DIC)

LABORATORY MANUAL

III / IV B.E. (ECE) : I – SEMESTER (R16)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL INTEGRATED CIRCUITS (DIC) - LAB

III / IV B.E. (ECE) : I - SEMESTER

LIST OF EXPERIMENTS

1. Realization of Gates by using Universal Building Blocks.
2. Minimization and Realization of a given function.
3. Realization of Flip-Flops.
4. Function generation by using Decoders & Multiplexers.
5. 4-bit Ripple counter.
6. Mod-8 Synchronous Counter.
7. 4-bit Shift Register.
8. 4 bit & 8-bit Binary Adders & Subtractors.
9. Seven Segment Display.
10. Priority encoding using 74LS148.
11. Arithmetic & Logic Unit (ALU).
12. Semi-Conductor Memory.
13. Applications of Multiplexer.
14. 4 – bit Comparator

Realization of gates by using

Universal Building Blocks

1. Realization of gates by using Universal Building Blocks

Aim : To Realize AND,OR,NOT,EX-OR and EX-NOR gates by using only NAND and only NOR gates

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7400	2
3.	IC 7402	2

Circuit Diagram :

Procedure :

Using NAND Gates

1. Derive truth table
2. Realize expression of AND gate by using number of NAND gates
3. Connect the circuit according to step?
4. Verify the truth table
5. Repeat above steps for OR, NOT, EX-OR and EX-NOR gates

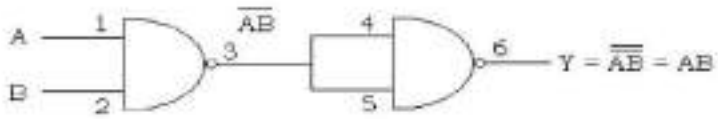
Using NOR Gates

1. 1. Derive truth table
2. Realize expression of AND gate by using number of NOR gates
3. Connect the circuit according to step?
4. Verify the truth table
5. Repeat above steps for OR, NOT, EX-OR and EX-NOR gates

Result :

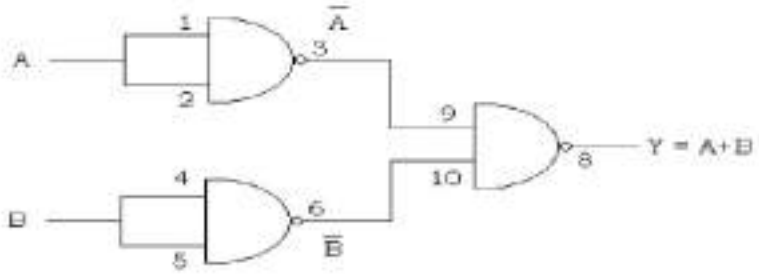
Basic gates are realized by using Universal building blocks.

Realization of AND gate using only NAND gates



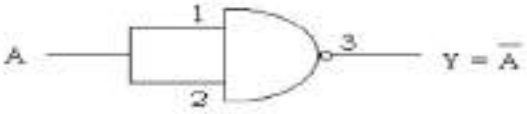
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

Realization of OR gate using only NAND gates



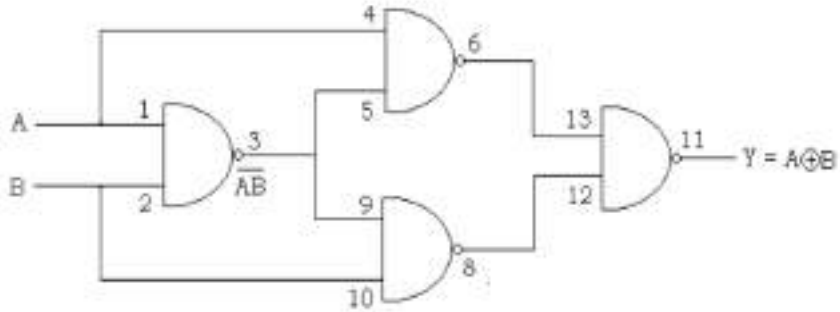
A	B	Y =A+B
0	0	0
0	1	1
1	0	1
1	1	1

Realization of NOT gate using only NAND gates



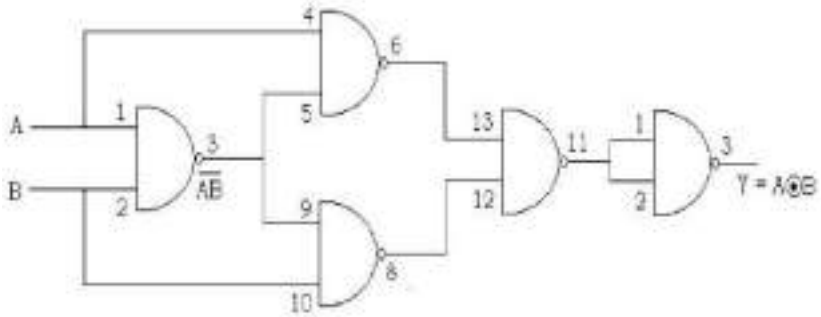
A	Y = A
0	1
1	0

Realization of EX-OR gate using only NAND gates



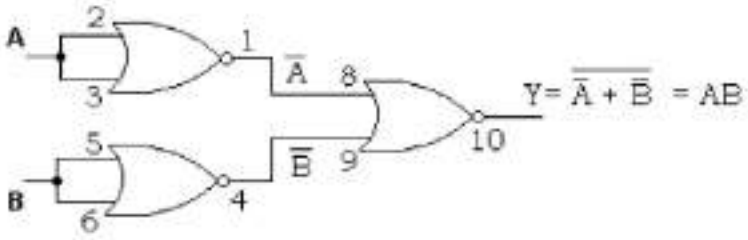
A	B	Y = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Realization of EX-NOR gate using only NAND gates



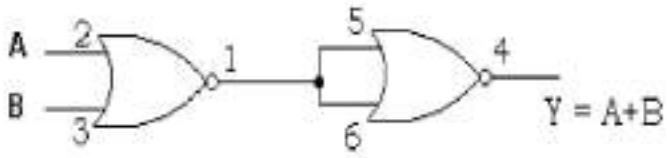
A	B	Y = A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

Realization of AND gate using only NOR gates



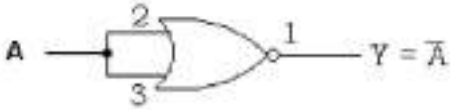
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

Realization of OR gate using only NOR gates



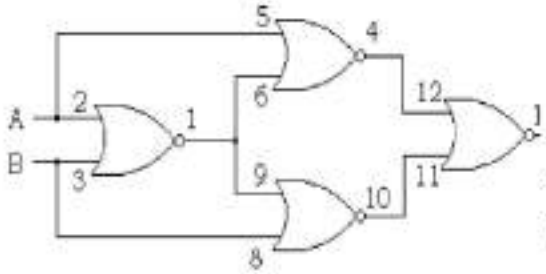
A	B	Y =A+B
0	0	0
0	1	1
1	0	1
1	1	1

Realization of NOT gate using only NOR gates

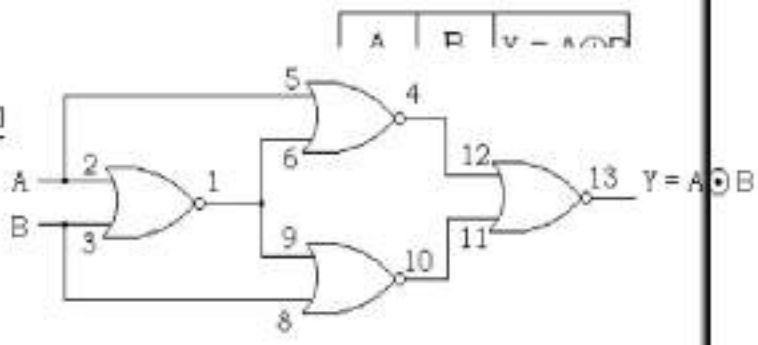


A	$Y = \bar{A}$
0	1
1	0

Realization of EX-OR gate using only NOR gates



Realization of EX-NOR gate using only NOR gates



A	B	Y = A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

Viva Questions :

1. Why NAND and NOR gates are called as Universal gates?
2. Realize NAND gate by using only NOR gates.
3. Realize NOR gate by using only NAND gates.
4. What are the applications of EX-NOR gate?
5. What is a logic gate?
6. Realize the given SOP expression by using only NAND and only NOR gates.
7. Realize the given POS expression by using only NAND and only NOR gates.
8. Show that NAND gate is equivalent to bubbled OR gate?
9. What do you mean by alphanumeric code? Name some of them? 10. Convert decimal number 24 into excess-3 number?

Minimization and Realization of a given function.

2. Minimization and Realization of a given Function

Aim : To minimize and realize a given function by using AND, OR, NOT and EX-OR gates.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7408	1
3.	IC 7432	1
4.	IC 7486	1
5.	IC 7404	1

Circuit Diagram :

Procedure :

1. First minimize the given expression.
2. Derive the truth table from the given function.
3. Realize the above simplified expression by using minimum number of gates.
4. Connect the circuit according to step 3.
5. Verify the truth table.

Result :

The given expression is minimized and realized by using different gates.

Viva Questions :

1. Design AND and OR gates by using switches.
2. What are duality properties?
3. What are Demorgan Laws?
4. What is a positive logic & negative logic system?
5. How do you identify the pins of an IC packages?
6. What is the difference between 7400 series & 5400 series ICs?
7. Show the truth table of negative logic AND gate.
8. State and prove consensus theorem and transposition theorem.
9. State commutative, associative, distributive, idempotence and absorption laws.
10. Write the truth tables for 3-input X-OR and X- NOR gates.
11. What is meant by self complementing code?
12. What do you mean by cyclic code? Give an example of a cyclic code
13. What is a parity bit? What do you mean by Odd and even parity systems?

Realization of Flip-Flops.

. Realization of Flip - Flops

Aim : To Construct different types of flip-flops and verify the truth tables.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	1
3.	IC 7400	1
4.	IC 7404	1

Circuit Diagram:

Procedure :

1. RS flip-flop is wired as shown in fig and input signals are fed from logic input switches and the out put is monitored on the logic level out put condition indicators and the truth table is verified.
2. JK flip-flop is wired as shown in fig and the input signals are fed from logic input switches and the output is monitored on the logic level output condition indicators and the truth table is verified.
3. Verify the truth tables of D flip flop and T flip flop in the same procedure.

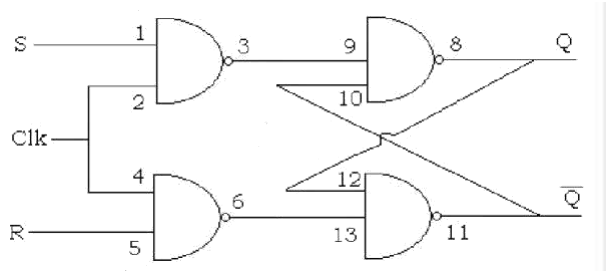
Result :

Truth tables of RS, JK, D and T flip-flops are verified.

Viva Questions :

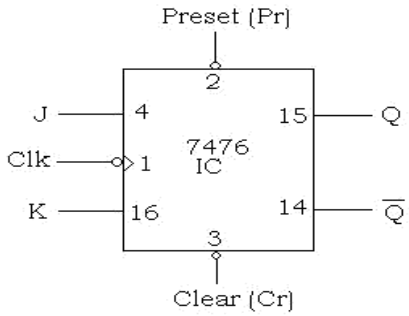
1. What is a flip-flop & latch?
2. What is a Race around condition in JK flip-flop?
3. How will you SET/CLEAR a flip-flop asynchronously?
4. What are the applications of T and D flip flops?
5. What is meant by positive edge triggering & negative edge triggering?
6. Distinguish between combinational circuit and sequential circuit
7. What is the difference between edge triggering and level triggering?
8. Define the Set-up time and Hold time of a flip-flop
9. Convert a T flip-flop in to D flip-flop
10. Realize RS flip-flop by using only NOR gates
11. How is the output frequency of a T flip-flop relates to the input frequency.

Realization of RS flip- flop using NAND gates



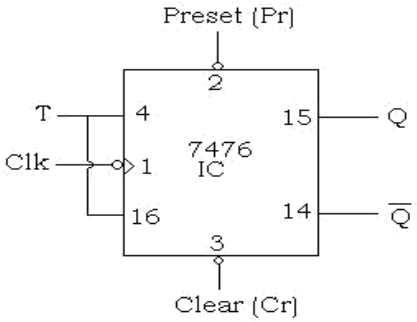
Clk	S	R	Theoretical Q_{n+1}	Practical Q_{n+1}
0	X	X	Q_n	
1	0	0	Q_n	
1	0	1	0	
1	1	0	1	
1	1	1	?	

JK flip- flop



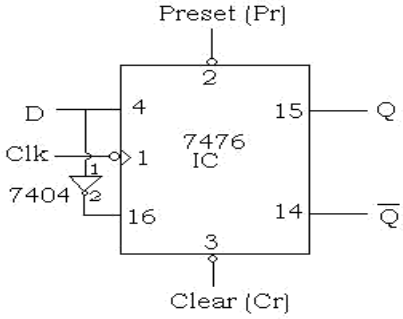
Clk	PR	CR	J	K	Theoretical Q_{n+1}	Practical Q_{n+1}
0	0	1	X	X	1	
0	1	0	X	X	0	
↓	1	1	0	0	Q_n	
↓	1	1	0	1	0	
↓	1	1	1	0	1	
↓	1	1	1	1	$\overline{Qn}$	

T flip- flop



Clk	PR	CR	T	Theoretical Q_{n+1}	Practical Q_{n+1}
0	0	1	X	1	
0	1	0	X	0	
↓	1	1	0	Q_n	
↓	1	1	1	$\overline{Qn}$	

D flip- flop



Clk	PR	CR	D	Theoretical Q_{n+1}	Practical Q_{n+1}
0	0	1	X	1	
0	1	0	X	0	
↓	1	1	0	0	
↓	1	1	1	1	

Function generation by using Decoders & Multiplexers.

4. Function generation by using Decoders & Multiplexers.

Aim : To implement given function by using decoders & multiplexers.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 74153	1
3.	IC 7442	1
4.	IC 7420	1
5.	IC 7421	1
6.	IC 7404	1

Circuit Diagram :

Procedure :

Using Decoders :

1. Obtain truth table from the given function
2. Realize the given function by using Decoders.
3. Connect the circuit according to step 2
4. Verify the truth table.

Using Multiplexer :

1. Obtain truth table from the given function.
2. Obtain canonical SOP from the given function.
3. Select size of the MUX depending on the no. of input variables.
4. Derive the implementation table.
5. Realize the given function by using MUX.
6. Connect the circuit according to step 5.
7. Verify the truth table.

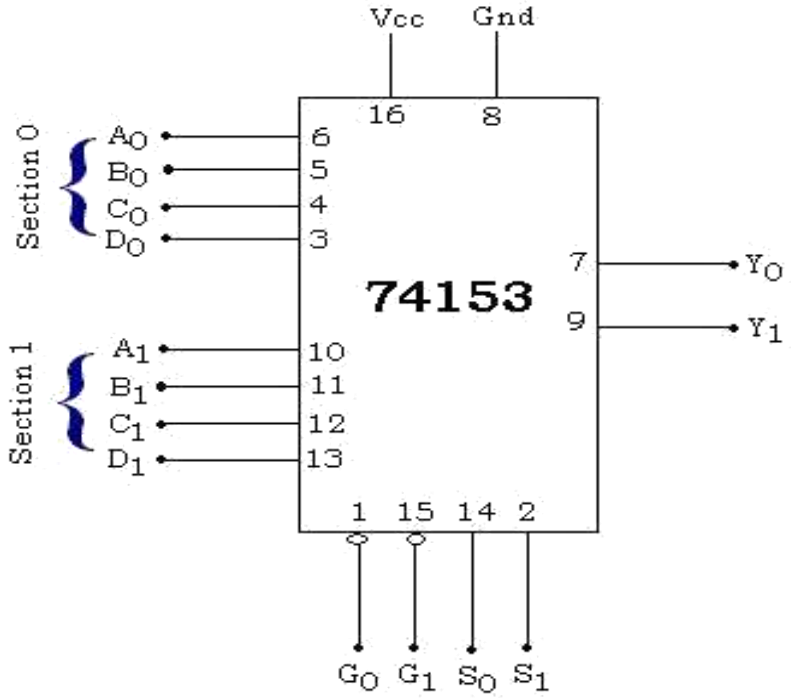
Result :

The given function is realized by using decoders & multiplexers.

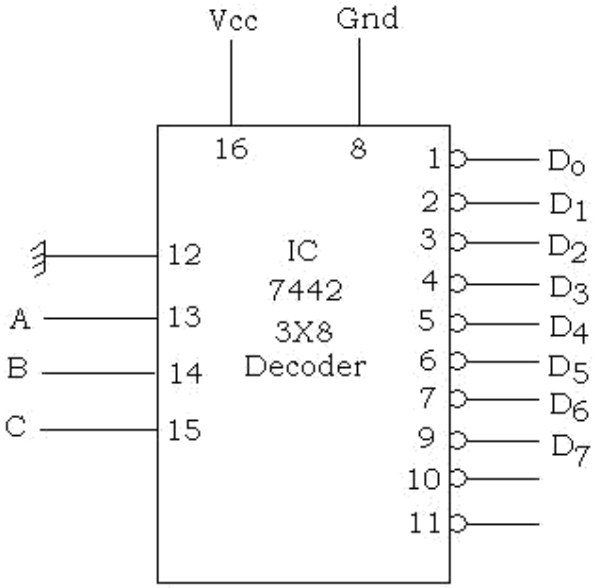
Viva Questions:

1. What is a MUX?
2. What are the applications of MUX?
3. What is a decoder?
4. What is the use of Enable input in Decoder?
5. What is the difference between MUX & DEMUX?
6. Realize full adder by using MUX.
7. Realize full subtractor by using Decoder.
8. Explain how a decoder can be used as a Demultiplexer?
9. Construct a parallel to serial converter using the MUX.
10. Construct a 64 x 1 MUX using 8 x 1 MUX.

Pin Diagram of 74153 MUX :



Pin Diagram of 7442 DECODER :



4-bit Ripple counter

5. 4-bit Ripple counter.

Aim : To design Asynchronous (Ripple) counter and verify the truth table.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	2

Circuit Diagram :

Procedure :

1. Ripple counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ1Q2Q3$ are observed and verify the truth table.

Result :

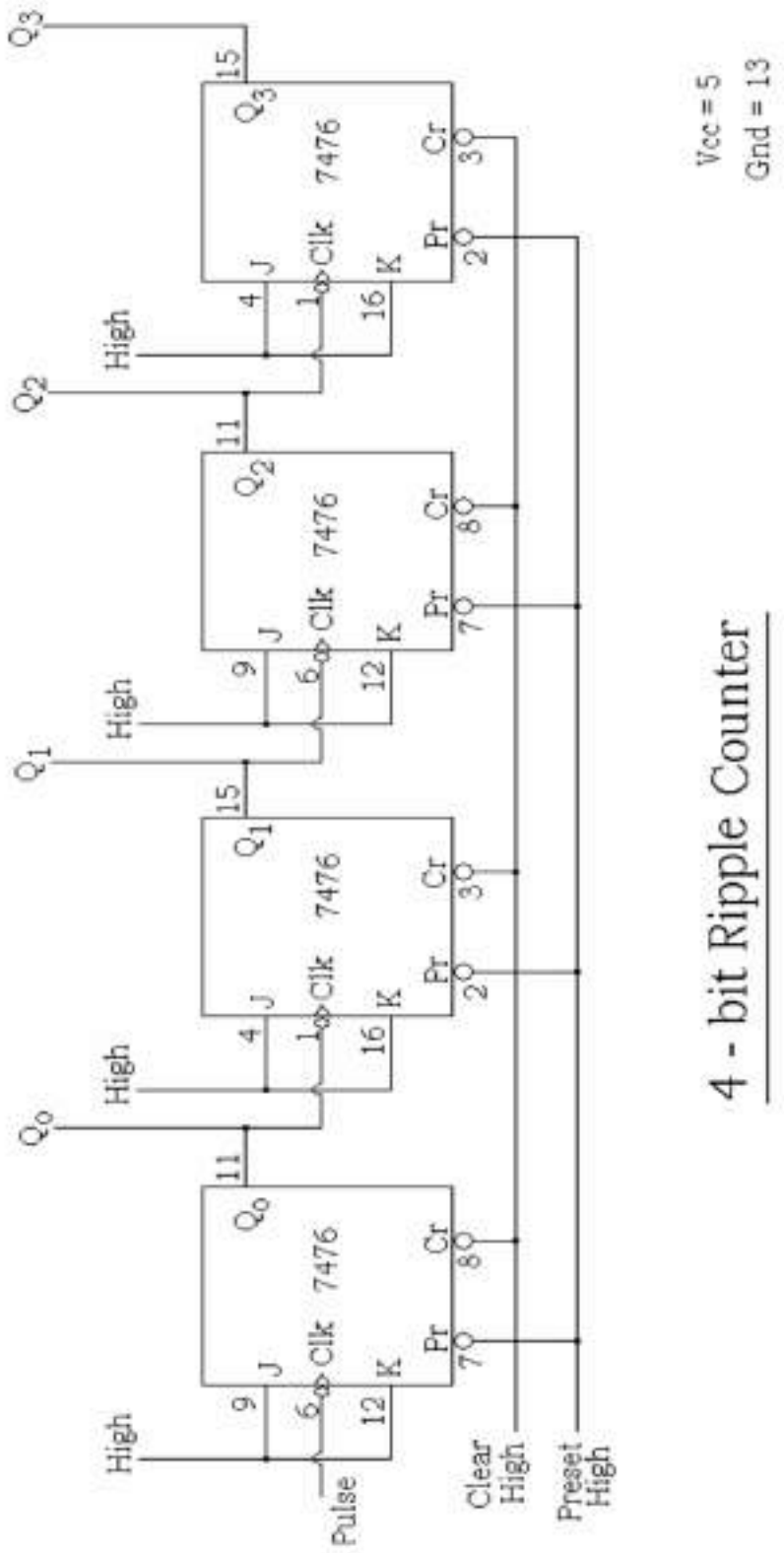
Asynchronous counter is constructed and truth table is verified.

Viva Questions :

1. What is the purpose of the counter?
2. What is the difference between Synchronous and Asynchronous Counters?
3. What is meant by “lockout” in counters?
4. What are the applications of the counters?
5. What is an excitation table?
6. What is the advantage of Ripple counter over Synchronous Counter?
7. What is the advantage of Synchronous counter over Ripple Counter?

4 – bit Ripple Counter Truth Table.

Clock pulses	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0


Q3
Q2
Q1
Q0
7476
J
Clk
K
Pr
Cr
High
Pulse
Clear
High
Preset
High
Vcc = 5
Gnd = 13
4 - bit Ripple Counter

Mod-8 Synchronous Counter

6. Mod-8 Synchronous Counter.

Aim : To design Mod-8 synchronous counter and verify the truth table.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	2
3.	IC 7408	1

Circuit Diagram :

Procedure :

1. Mod- 8 Synchronous counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ_1Q_2Q_3$ are observed and verify the truth table.

Result :

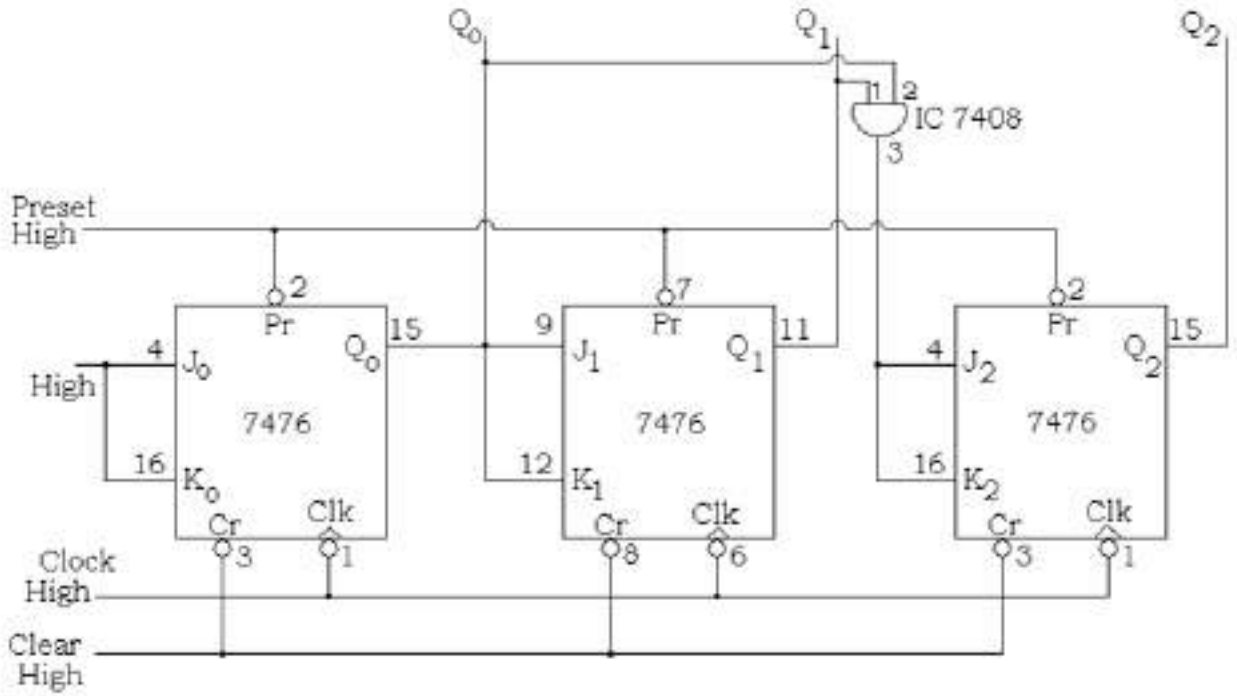
Mod - 8 Synchronous counter is constructed and truth table is verified.

Viva Questions:

1. What do you mean by the self starting type counter?
2. What do you mean by the modulus of a counter?
3. What is the difference between a BCD counter and Decade counter
4. What is the maximum modulus of a counter with 'n' flip-flops?
5. What are the invalid states in the BCD COUNTER?
6. What do you mean by a presettable counter?

Mod-8 Synchronous Counter Truth Table :

Clock pulses	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



IC 7476 Vcc = 5 Gnd = 13

IC 7408 Vcc = 14 Gnd = 7

Mod - 8 Synchronous Counter

4 – bit Shift Register

7. 4 - bit Shift-Register

Aim : To design 4-bit shift register and verify the operation of serial loading and parallel loading,

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7474	2
3.	IC 7400	1

Circuit Diagram :

Procedure :

1. Connect the circuit as shown in fig.
2. For serial loading keep load low.
3. First clear all the flip-flops by supplying clear = low
4. First enter serial input one by one, through clock pulse; we will get parallel output at $Q_3Q_2Q_1Q_o$. After applying 4 clock pulses we will get serial output.
5. For parallel input keep load = high
6. Directly apply parallel input to $P_{r3}, P_{r2}, P_{r1}, P_{r0}$; we will get parallel output at $Q_3Q_2Q_1Q_o$. After applying 4 clock pulses we will get serial output.

Result : The operation of 4-bit shift register for serial loading and parallel loading is observed

Viva Questions :

1. What do you mean by shift register?
2. Explain the operation of a left shift register & a right shift register?
3. How will you use a shift register to multiply or divide a binary number by 2?
4. List the Shift Register ICs.
5. What is the difference between a register and shift register?
6. What is the difference between a ring counter and a Johnson counter
7. What is meant by universal shift register?
8. Explain the various modes in which the data can be entered or taken out from a register?

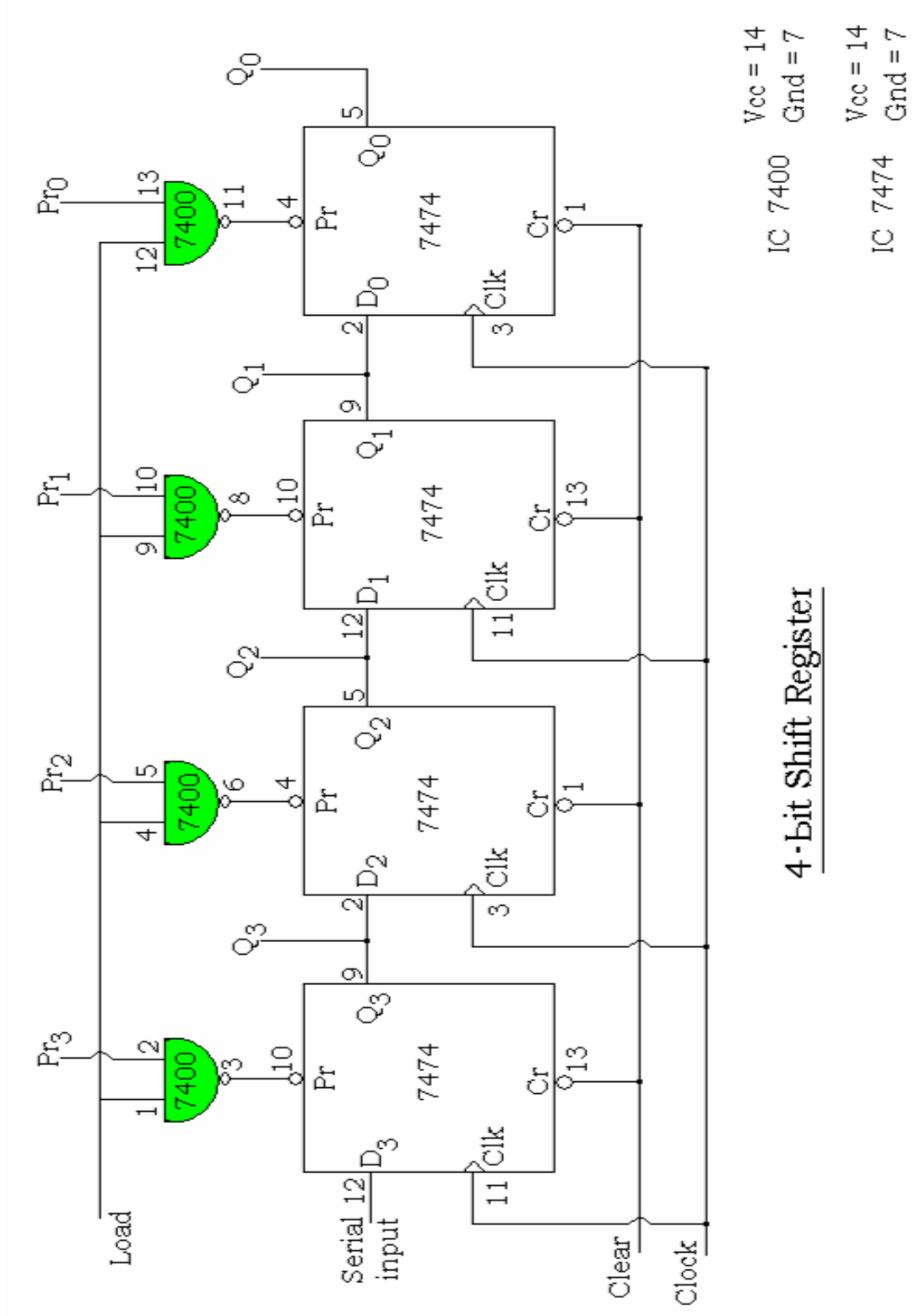
4 – bit Shift Register Truth Table :

Serial Input → Serial Output / Parallel Output : The input is 1010.

Load	Clk	Clear	Serial i/p	Parallel output				Serial output Qo
				Q3	Q2	Q1	Q0	
0	X	0	X	0	0	0	0	0
0	1	1	0	**0**	0	0	0	0
0	2	1	1	**1**	**0**	0	0	0
0	3	1	0	**0**	**1**	**0**	0	0
0	4	1	1	**1**	**0**	**1**	**0**	**0**
0	5	1	0	0	1	0	1	**1**
0	6	1	0	0	0	1	0	**0**
0	7	1	0	0	0	0	1	**1**

Parallel input → Parallel Output / Serial Output : The input is 1010.

Load	Clk	Clear	Parallel i/p				Parallel output				Serial output Qo
			Pr3	Pr2	Pr1	Pr0	Q3	Q2	Q1	Q0	
0	X	0	X	X	X	X	0	0	0	0	0
1	X	1	1	0	1	0	**1**	**0**	**1**	**0**	**0**
0	1	1	X	X	X	X	0	**1**	**0**	**1**	**1**
0	2	1	X	X	X	X	0	0	**1**	**0**	**0**
0	3	1	X	X	X	X	0	0	0	**1**	**1**


4-bit Shift Register
IC 7400 Vcc = 14 Gnd = 7
IC 7474 Vcc = 14 Gnd = 7
7400
7474
Pr
Cr
Clk
D0
D1
D2
D3
Q0
Q1
Q2
Q3
Pr0
Pr1
Pr2
Pr3
Load
Serial input
Clear
Clock

4 bit & 8-bit Binary Adders & Subtractors.

8. 4 bit & 8-bit Binary Adders & Subtractors.

Aim : To construct and evaluate 4 bit and 8 bit adders and subtractors

Apparatus and Components :

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 7483	2
3.	IC 7486	2
4	IC 7404	1

Circuit Diagram :

Procedure :

Adders:

1. The circuit is connected as shown in fig.
2. Apply two 4 bit positive numbers A and B, observe the output.
3. Verify the truth table.
4. Repeat above steps for 8 bit adders also.

Subtractors :

1. The circuit is connected as shown in fig
2. Apply two 4 bit positive numbers A and B represented in sign magnitude form, observe output which is also in sign magnitude form,
3. Verify the truth table

Result :

The truth tables for 4 bit & 8 bit full adders and subtractors are verified

Viva Questions :

1. Describe the operation performed by the following circuits
   a) Half-Adder, b) Full-Adder, c) Half-Subtractor, d) Full-Subtractor.
2. What is the difference between ripple carry adder and look ahead carry adder.
3. Compare serial and parallel binary adders.
4. How many full adders are required to construct a 4-bit parallel binary adder/subtractor.
5. Design a half adder using only NOR gates
6. Draw the block diagram of full adder by using half-adders
7. Design a full adder using only NAND gates.
8. Draw a circuit for adding BCD numbers and discuss its working.
9. What are the rules for mod-2 addition?
10. What are the rules for excess-3 addition?

Truth Table :

4 – bit Binary Subtractor :

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{in}	Sign	S_3	S_2	S_1	S_0

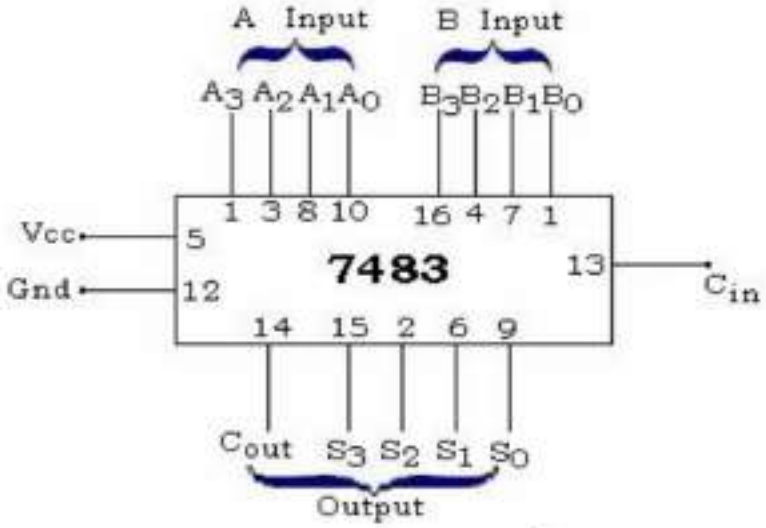
4 – bit Binary Adder :

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{in}	S_3	S_2	S_1	S_0	C_{out}

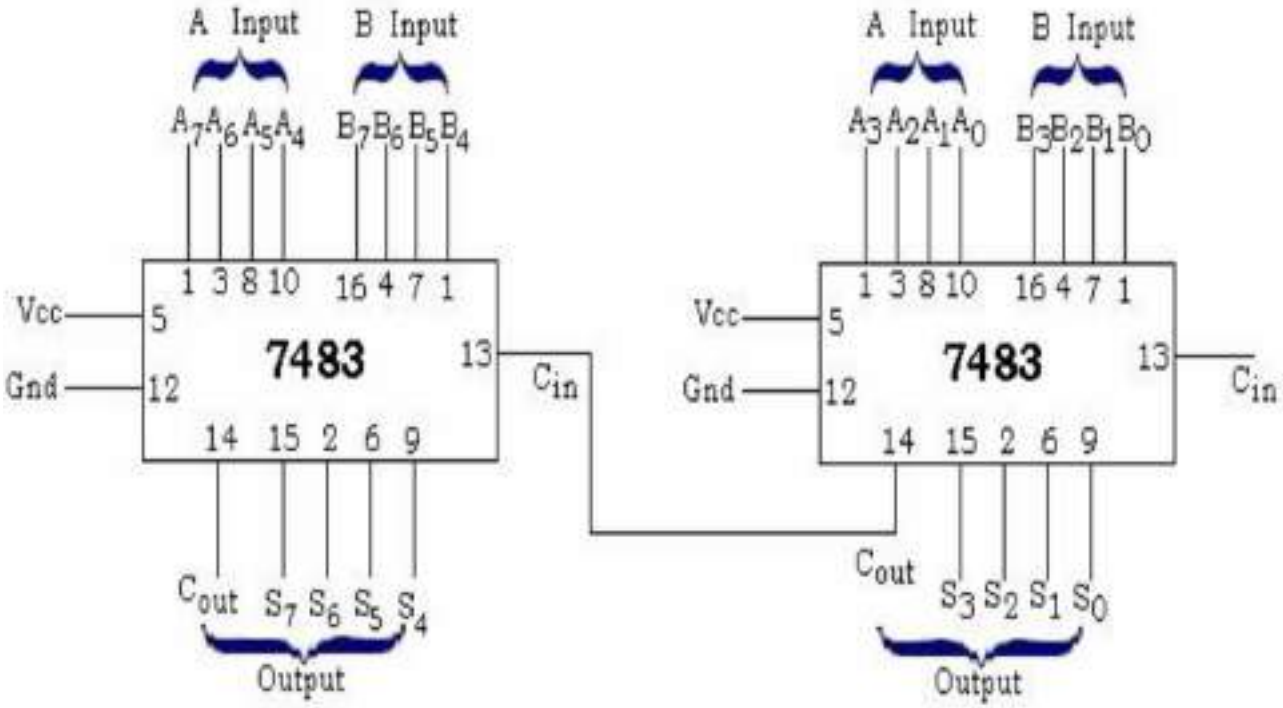
8 – bit Binary Adder :

A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Cin	S7	S6	S5	S4	S3	S2	S1	S0	Cout

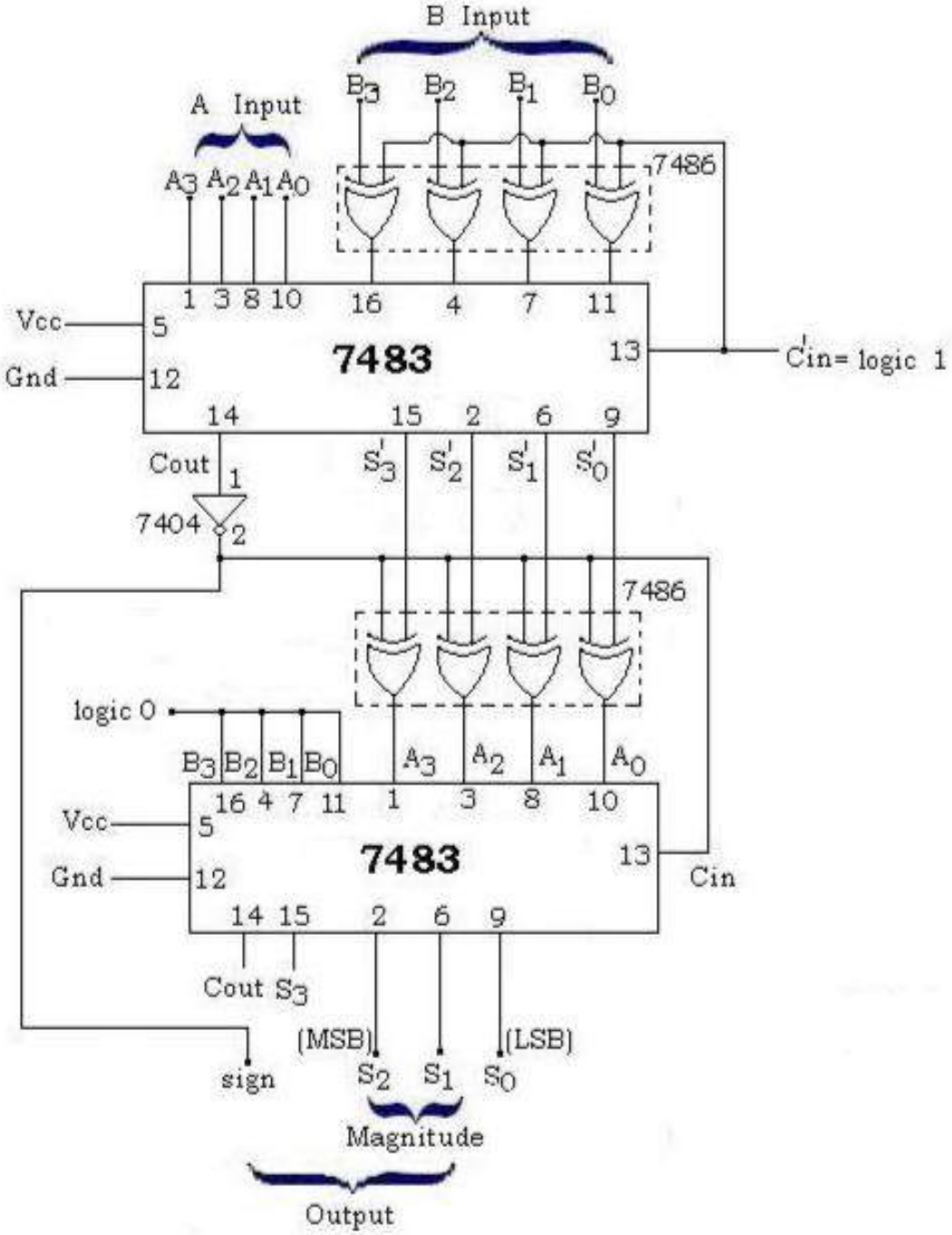
Circuit Diagram:



4 - bit Adder



8 - bit Adder



4- bit Subtractor

Seven Segment Display

9. Seven Segment Display

Aim : To study BCD to Seven - Segment decoder.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 7447	1
3.	IC FND 507	1

Circuit Diagram :

Procedure :

1. Set up the Ckt as shown in fig.
2. Apply logic '0' level to LT and observe the seven segments of the LED. All the segments must be ON.
3. Apply logic '0' level to BI/RBO and observe the seven segments of the LED. All the segments must be OFF.
4. Apply logic '1' to LT and RBI and observe the number displayed on the LED for all the inputs 0000 through 1111. This is the normal decoding mode.
5. Apply logic '1' to LT and logic '0' to RBI, and observe the BI/RBO output and the number displayed on the LED for all the inputs 0000 through 1111. This is the normal decoding mode with zero blanking.

The functions of LT, RBI, RBO and BI are given below.

LT This is called the LAMP TEST terminal and is used for segment testing. If it is connected to logic '0' level, all the segements of the display connected to the decoder will be ON. For normal decoding operation, this terminal is to be connected to logic '1' level.

RBI For normal decoding operation, this is connected to logic '1' level. If it is connected to logic '0', the segment outputs will generate the data for normal 7-segment decoding, for all BCD inputs except Zero. Whenever the BCD inputs correspond to Zero, the 7-segment display switches off. This is used for zero blanking in multi-digit displays.

BI If it is connected to logic '0' level, the display is switched-off irrespective of the BCD inputs. This is used for conserving the power in multiplexed displays.

RBO This output is used for cascading purposes and is connected to the RBI terminal of the succeeding stage.

Result :

The operation of BCD to SEVEN SEGMENT display is verified.

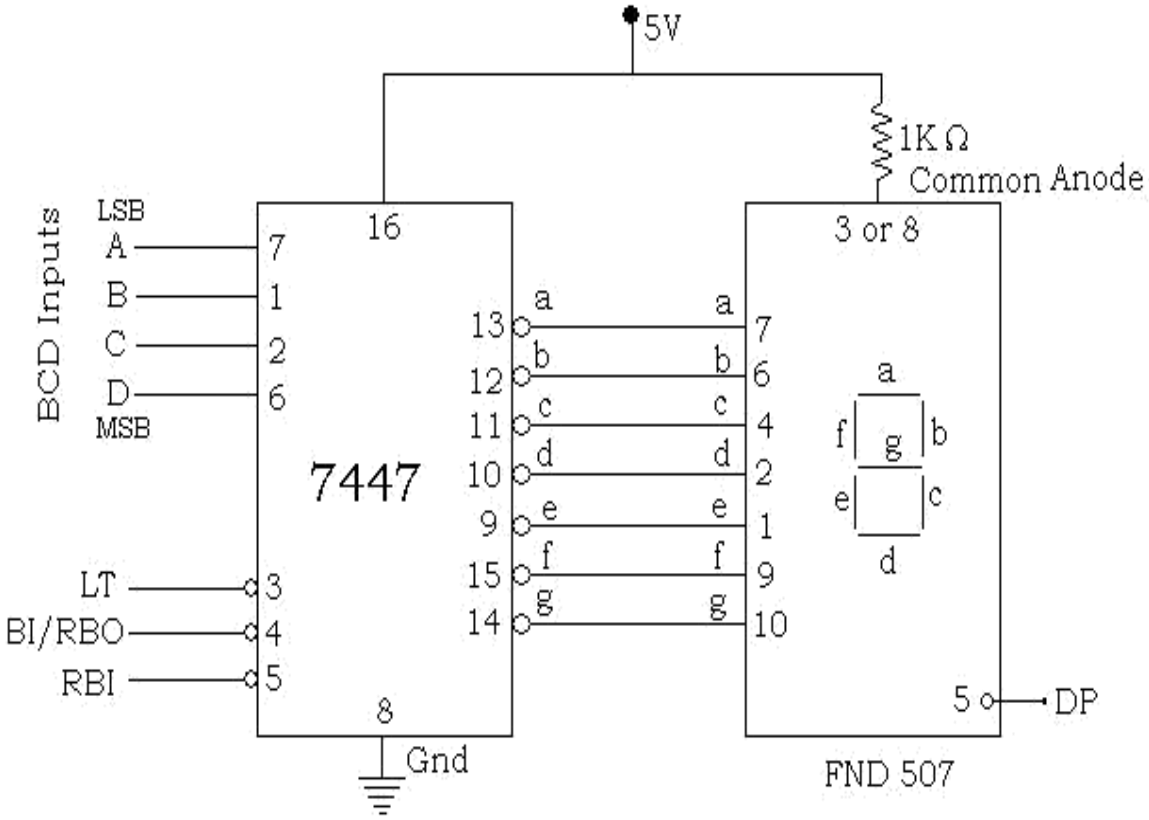
Truth Table :

D	C	B	A	a	b	c	d	e	f	g	Display Number
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

Viva Questions :

1. What are the applications of seven segment display?
2. Can you use the segments outputs of 7448 decoder directly to drive a 7-Segment LED? If not suggest a suitable interface
3. What is the difference between common anode & common cathode display?
4. Describe the operation performed by the decoder?
5. What is the function of RBI input?
6. What is the number of inputs and outputs of a decoder that accepts 64 different input combinations?
7. Explain how a BCD to Decimal decoder can be used as a 3 to 8 decoder.
8. What is the function of LT input?
9. What is the function of BI/RBO pin?

Circuit Diagram



Priority Encoding using 74LS148.

10. Priority Encoding using 74LS148.

Aim : To study octal to binary encoder.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 74148	1

Circuit Diagram :

Procedure :

1. Connect as per the Ckt diagram.
2. Apply high value to (pin 10) octal input zero remaining all seven octal inputs to low value (0) observe the output, CBA = 111
3. Repeat the step 2; up to 7 octal inputs and observe the outputs
4. Verify practically the given tabular form.

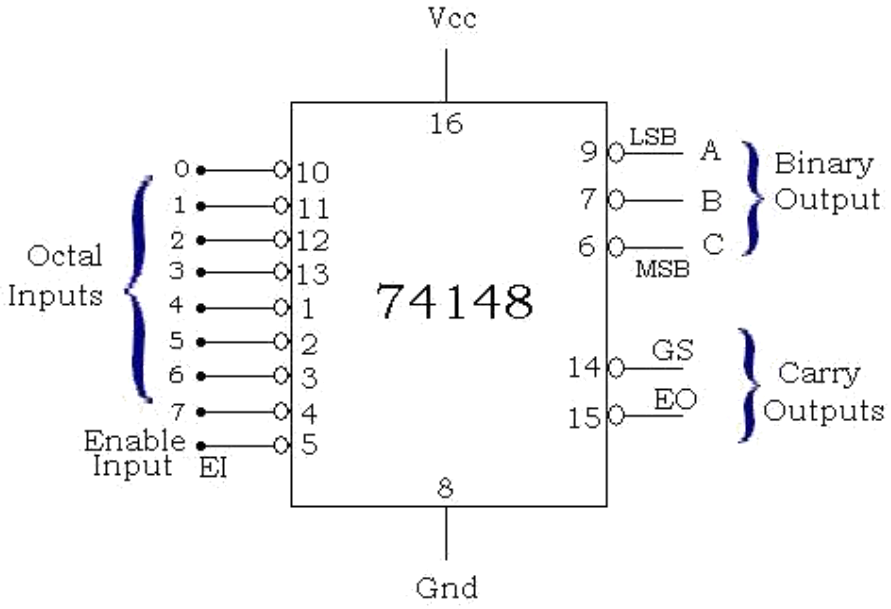
Result :

The operation of octal to binary encoder is verified.

Viva Questions :

1. How does a priority encoder differ from an ordinary encoder?
2. What is use of the ENABLE input in an encoder?
3. Describe the operation performed by the encoder
4. Draw the circuit of decimal to BCD encoder

Circuit Diagram :



Truth Table :

EI	Inputs								Outputs				
	0	1	2	3	4	5	6	7	C	B	A	GS	EO
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	X	0	1	1	1	1	1	1	1	1	0	0	1
0	X	X	0	1	1	1	1	1	1	0	1	0	1
0	X	X	X	0	1	1	1	1	1	0	0	0	1
0	X	X	X	X	0	1	1	1	0	1	1	0	1
0	X	X	X	X	X	0	1	1	0	1	0	0	1
0	X	X	X	X	X	X	0	1	0	0	1	0	1
0	X	X	X	X	X	X	X	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

Arithmetic & Logic Unit

11. Arithmetic & Logic Unit

Aim : To study arithmetic logic unit for performing the Logical & Arithmetic operations .

Apparatus and Components :

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 74181	1

Circuit Diagram :

Procedure :

Logical Operations :

1. Setup the circuit of 74181 IC for logical operation (M=1)
2. Apply the signals at the selection lines one by one.
3. Verify the logical operations performed on two binary data inputs A & B

Arithmetic Operations :

1. Setup the circuit for arithmetic operation (M=O)

a) Addition :

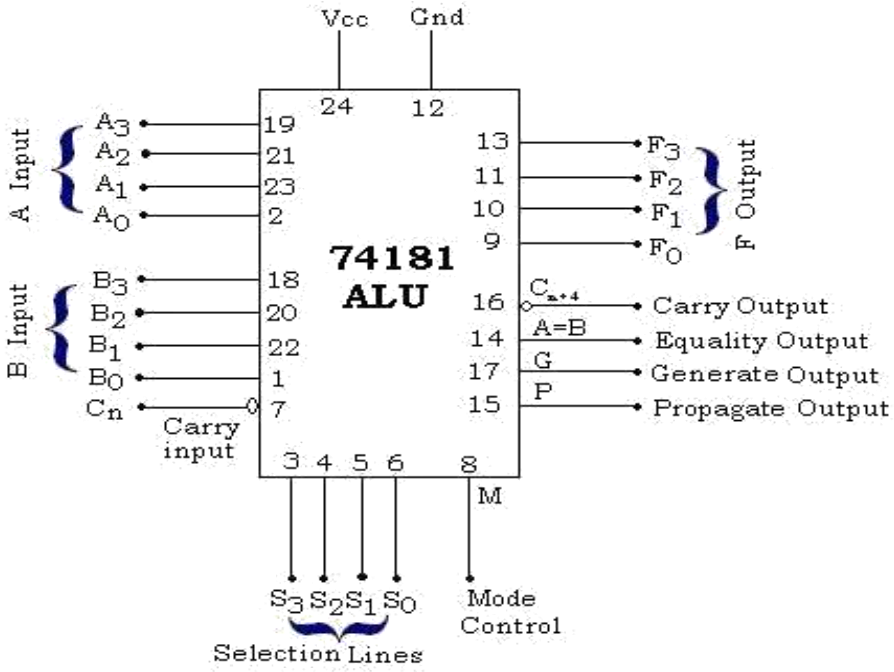
Refer line (9) of table; apply 1001 signals at selection lines. For data inputs A&B, observe the outputs at C_{n+4}, F3, F2, F1 and F0 for a) Cn = 1 (no carry) and b) Cn = 0 (with carry). The results will be a 5-bit binary word expressed as C_{n+4} F3 F2 F1 F0.

b) Subtraction:

Refer line (6) of table; apply 0110 at the selection lines. For data inputs A and B observe the out puts at C_{n+4}, F3, F2, F1 and F0 for (a) Cn = 1(no carry) and (b) Cn = o (with carry). The result is expressed in sign-magnitude form. The C_{n+4} outputs give the sign; it is 0 for positive result and 1 for negative result. F3 F2 F1 F0 gives the magnitude, directly for positive result, and in 2's complement form for negative result.

Result : The operation of ALU is verified.

Circuit Diagram :



Function Table :

Sl. No	Selection Lines S3 S2 S1 S0	Active High Data		
		M = 1 Logic Functions	M = 0 Arithmetic Operations	
		C_n = X	C_n = 1 (no carry)	C_n = 0 (with carry)
0	0 0 0 0	F = $\overline{A}$	F = A	F=APLUS1
1	0 0 0 1	F = $\overline{A+B}$	F=A+B	F=(A+B)PLUS1
2	0 0 1 0	F = $\overline{A}$ .B	F=A+ $\overline{B}$	F=(A+ $\overline{B}$) PLUS 1
3	0 0 1 1	F = 0	F = MINUS 1	F = ZERO
4	0 1 0 0	F = $\overline{AB}$	F=APLUSA $\overline{B}$	F=APLUSA $\overline{B}$ PLUS 1
5	0 1 0 1	F = B	F = (A+B) PLUS A $\overline{B}$	F = (A+B) PLUS A $\overline{B}$ PLUS 1
6	0 1 1 0	F=A⊕B	F = A MINUS B MINUS 1	F=AMINUSB
7	0 1 1 1	F = A $\overline{B}$	F = A $\overline{B}$ MINUS 1	F = A $\overline{B}$
8	1 0 0 0	F = $\overline{A}$ + B	F=APLUS AB	F = A PLUS AB PLUS 1
9	1 0 0 1	F = $\overline{A \oplus B}$	F=APLUS B	F=APLUS BPLUS1
10	1 0 1 0	F = B	F=(A+ $\overline{B}$) PLUS AB	F=(A+ $\overline{B}$) PLUS AB PLUS 1
11	1 0 1 1	F=AB	F = AB MINUS 1	F=AB
12	1 1 0 0	F = 1	F=APLUS A	F=APLUS APLUS1
13	1 1 0 1	F=A+ $\overline{B}$	F = (A+ B) PLUS A	F=(A+B)PLUS APLUS1
14	1 1 1 0	F=A+B	F=(A+ $\overline{B}$) PLUS A	F=(A+ $\overline{B}$) PLUS A PLUS 1
15	1 1 1 1	F = A	F=AMINUS1	F = A

Semi-Conductor Memory.

12. Semi-Conductor Memory.

Aim: To verify Read and Write operations of memory IC 7489 RAM.

Apparatus and Components :

S.No	Name	Range / Value	Quantity
1.	Bread board		1
2.	Fixed regulated power supply	5V	1
3.	IC 7489		1
4.	Resistors	1K	4
5.	LED		4

Circuit Diagram:

Procedure:

To Write into any memory location:

1. Connect the circuit as shown in fig.
2. Apply the address of the chosen memory location at the address I/P terminals.
3. Apply the data to be stored at the data I/P terminals.
4. Apply Logic 0 at the R/$\overline{W}$ line.
5. Change CE from logic 1 to logic 0.

To Read from any memory location:

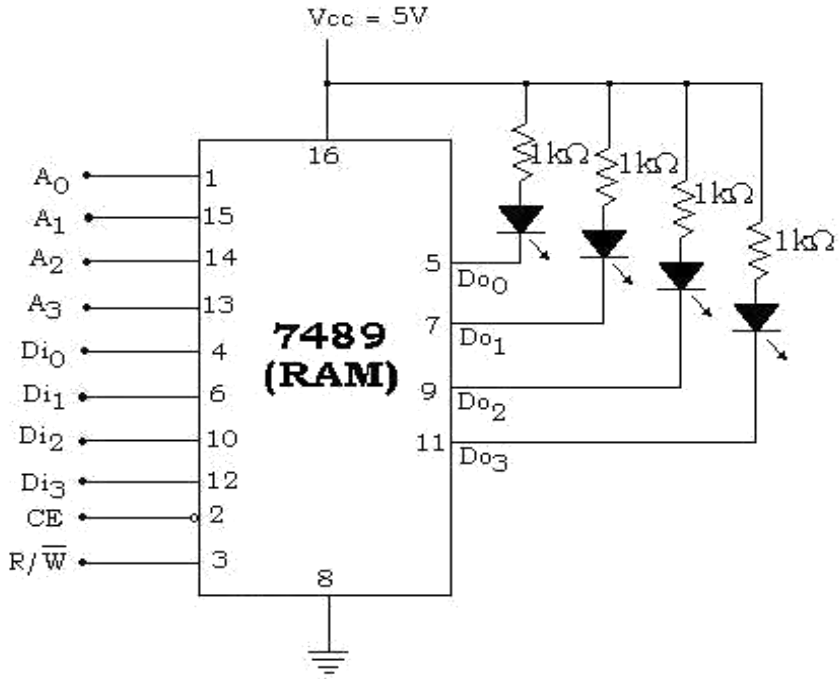
1. Connect the circuit as shown in fig.
2. Apply the address of the chosen memory location at the address I/P terminals.
3. Apply Logic 1 at the R/$\overline{W}$ line.
4. Change CE from logic 1 to logic 0.

Result: Read and Write operations of memory are verified.

Viva Questions:

1. What is a RAM?
2. What is a ROM?
3. What do you mean by PROM?
4. What do you mean by EPROM?
5. What are the merits and demerits of Dynamic memory over Static memory?
6. What is the difference between volatile memory and non-volatile memory?
7. What is the difference between sequential access and random access?
8. What is meant by refreshing of the memory?
9. Describe the advantages of an EEPROM over an EPROM
10. How many address inputs, Data inputs and Data outputs are required for a 32K x 12 Memory?
11. Define access time of a memory?

Circuit Diagram:



Truth Table :

For WRITE Operation

CE	R/$\overline{W}$	Input Lines		Data Output Lines
		Address	Data	
		A0 A1 A2 A3	Di0 Di1 Di2 Di3	Do0 Do1 Do2 Do3
0	0	0 0 0 0		
0	0	0 0 0 1		
0	0	0 0 1 0		
0	0	0 0 1 1		
0	0	0 1 0 0		
0	0	0 1 0 1		
0	0	0 1 1 0		
0	0	0 1 1 1		
0	0	1 0 0 0		
0	0	1 0 0 1		
0	0	1 0 1 0		
0	0	1 0 1 1		
0	0	1 1 0 0		
0	0	1 1 0 1		
0	0	1 1 1 0		
0	0	1 1 1 1		

For READ Operation

CE	R/$\overline{W}$	Input Lines		Data Output Lines
		Address	Data	
		A0 A1 A2 A3	Di0 Di1 Di2 Di3	Do0 Do1 Do2 Do3
0	1	0 0 0 0		
0	1	0 0 0 1		
0	1	0 0 1 0		
0	1	0 0 1 1		
0	1	0 1 0 0		
0	1	0 1 0 1		
0	1	0 1 1 0		
0	1	0 1 1 1		
0	1	1 0 0 0		
0	1	1 0 0 1		
0	1	1 0 1 0		
0	1	1 0 1 1		
0	1	1 1 0 0		
0	1	1 1 0 1		
0	1	1 1 1 0		
0	1	1 1 1 1		

Applications of Multiplexer.

13. Applications of Multiplexer.

AIM: To verify the applications of multiplexer as i) Parallel to serial data converter. ii) Even and odd parity generator.

APPARATUS and COMPONENTS:

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 74151A	1

CIRCUIT DIAGRAM:

PROCEDURE:

Parallel to Serial data converter:

1. Select size of the multiplexer depending on the number of parallel inputs.
2. Connect the circuit as shown in the fig.
3. Apply logic '0' at the strobe input line.
4. Apply parallel data at the inputs of the multiplexer.
5. Apply 000 signals at the selection lines. In this case, the output of the multiplexer will be Ao.
6. Vary the signals at the selection lines from 001 to 111. Depending upon the code applied at the selection lines, one out of the parallel data A1,A2.....A7 is selected and transmitted to the output line.

Even parity generator:

1. Connect the circuit as shown in fig.
2. Prepare truth table for a three input even parity generator.
3. Apply even parity bits at the inputs of the multiplexer
4. Apply a 3-bit data word to the select terminals and observe the output.
5. Even parity of the data word is available at pin 5 and odd parity is available at pin 6.

RESULT: Application of multiplexer is observed as a parallel to serial data converter and even / odd parity generator.

Truth Tables :

Parallel To Serial Data Converter :

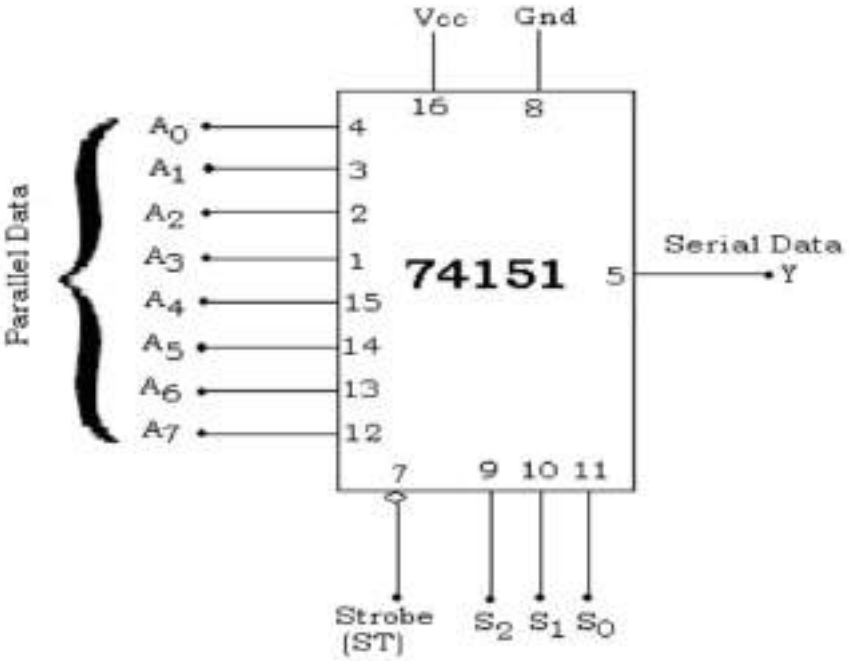
Parallel Data : (A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0) =

Selection Lines			Serial Data
S2	S1	S0	
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

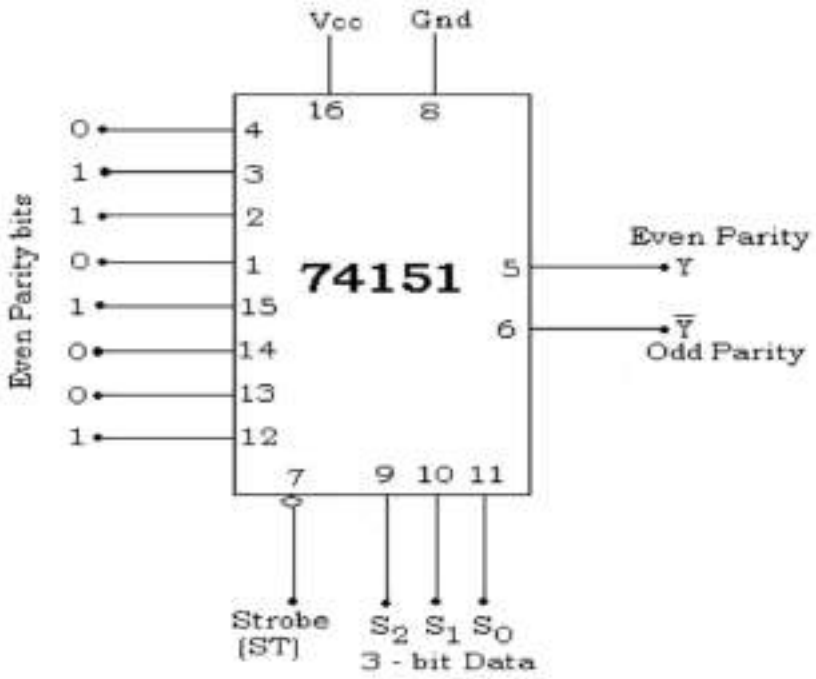
Even / Odd Parity Generator :

Data Inputs			Even Parity (bit)	Odd Parity (bit)
A	B	C		
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

CIRCUIT DIAGRAM:



Parallel to Serial Data Converter



Even / Odd parity Generator

4 – bit Magnitude Comparator

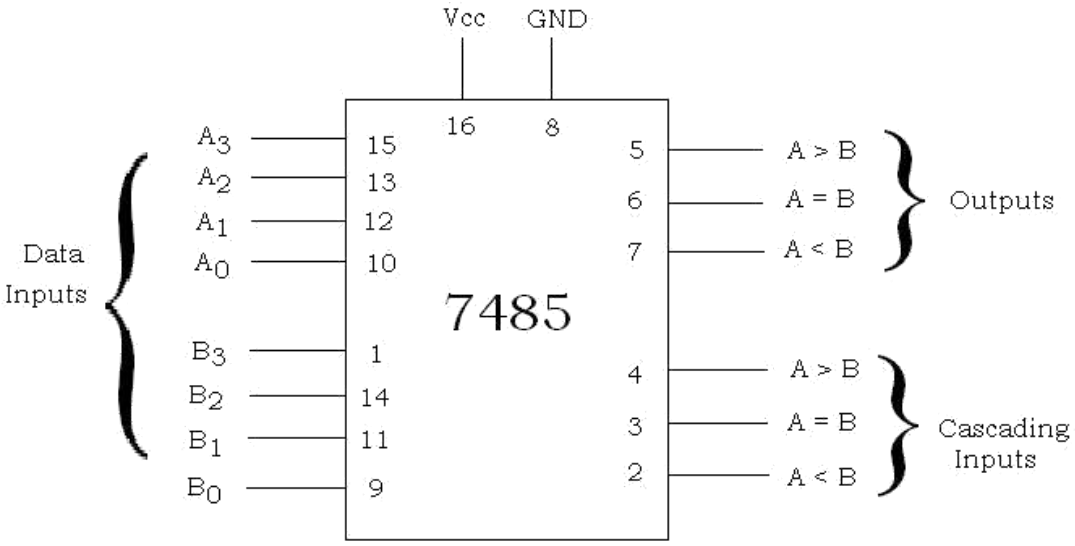
14. 4 – Bit Magnitude Comparator

AIM: To Compare two 4 – bit binary Numbers.

APPARATUS and COMPONENTS:

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 7485	1

CIRCUIT DIAGRAM:



PROCEDURE:

1. The circuit is connected as shown in fig.
2. Apply two 4 bit binary numbers A and B, observe the output.
3. Verify the truth table.
4. Repeat the above steps for different inputs.

RESULT: The magnitude of two 4 – bit binary numbers are compared.

Function Table :

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	**A2, B2**	**A1,B1**	**A0, B0**	**A > B**	**A < B**	**A = B**	**A > B**	**A < B**	**A = B**
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	1	1	0	0	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	0	1	1	0