Code No: **R1631043** **R16** SET - 1

III B. Tech I Semester Supplementary Examinations, August - 2021

DIGITAL IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A **(14 Marks)**

1. a) Give the logic levels and noise margins of TTL families. [2M]
b) What are the operators available in VHDL? [2M]
c) Define and explain Next statement. [2M]
d) What are advantages of Floating-Point Encoder? [3M]
e) List the various IC versions of shift registers. [3M]
f) Distinguish between Mealy and Moore Machines. [2M]

PART –B **(56 Marks)**

2. a) Explain the terms: i) Power consumption in CMOS; ii) Fan-out with reference to TTL gate. [7M]
b) What are the advantages and disadvantages of ECL? [7M]

3. a) Explain about levels of abstraction in VHDL. [7M]
b) Discuss the binding. Discuss the binding between entity and components. [7M]

4. a) Explain the structure of various LOOP statements in VHDL with examples. [7M]
b) Discuss about Signal Drivers. [7M]

5. a) With the help of logic diagram explain 74×157 multiplexer. Write the data flow Style VHDL program for this IC. [7M]
b) Write VHDL code for Barrel Shifter along with diagram. [7M]

6. a) Write down the VHDL code for a J-K flip flop. [7M]
b) Draw the circuit of a bidirectional shift register with parallel loading using 2-to-4-line decoder and D-flip-flops. [7M]

7. a) What is meant by finite state machine? What are the capabilities and limitations of finite state machine? [7M]
b) Convert the following mealy machine into a corresponding Moore machine. [7M]

P.S	NS,X=0	Z, X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0

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